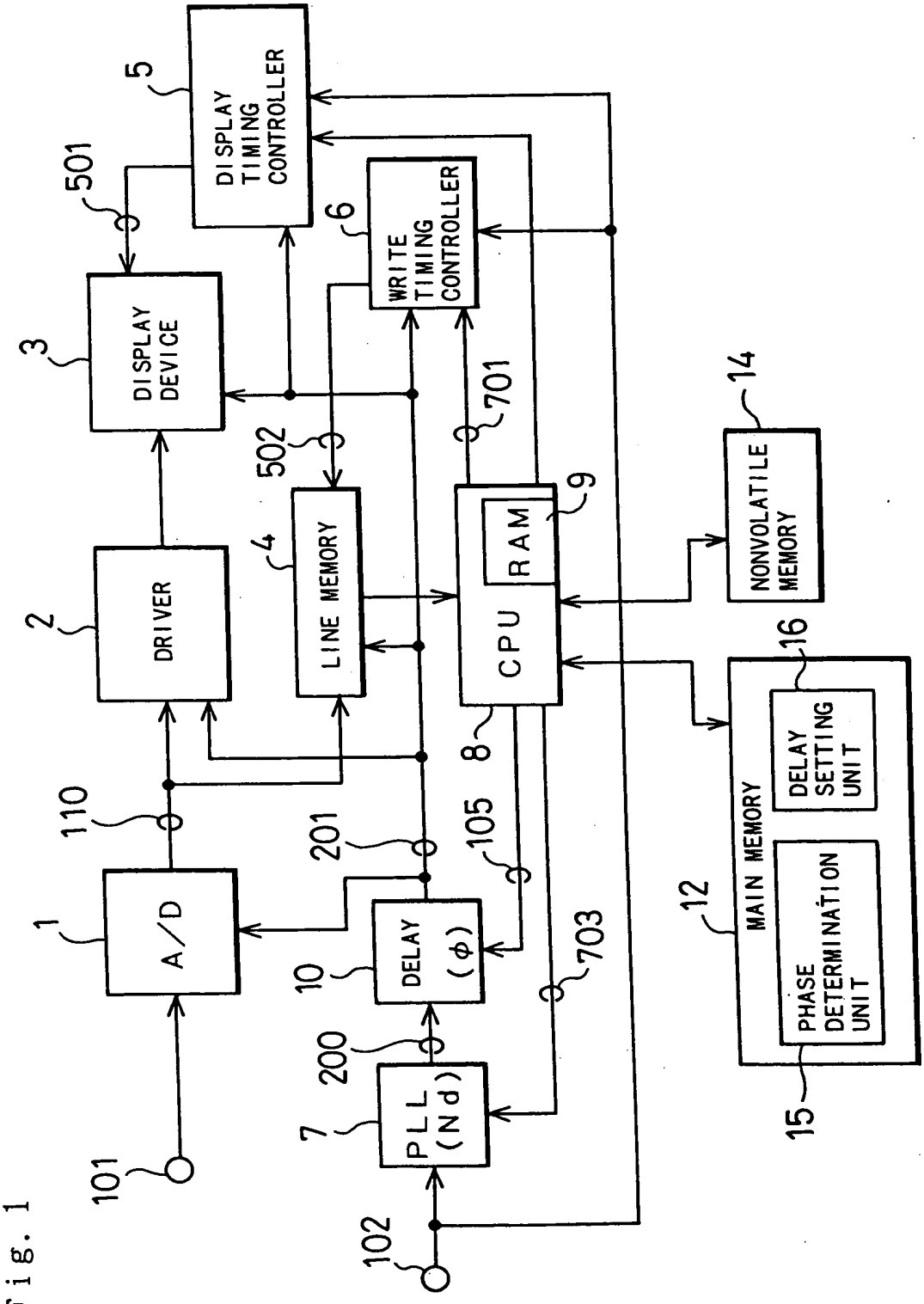

DISPLAY TIMING CONTROLLER
5
501
WRITE TIMING CONTROLLER
6
DISPLAY DEVICE
3
701
14
NONVOLATILE MEMORY
502
LINE MEMORY
4
RAM
9
DRIVER
2
CPU
8
16
DELAY SETTING UNIT
110
201
105
MAIN MEMORY
12
A/D
1
DELAY (φ)
10
PHASE DETERMINATION UNIT
703
200
PLL (Nd)
7
15
101
102

Fig. 1

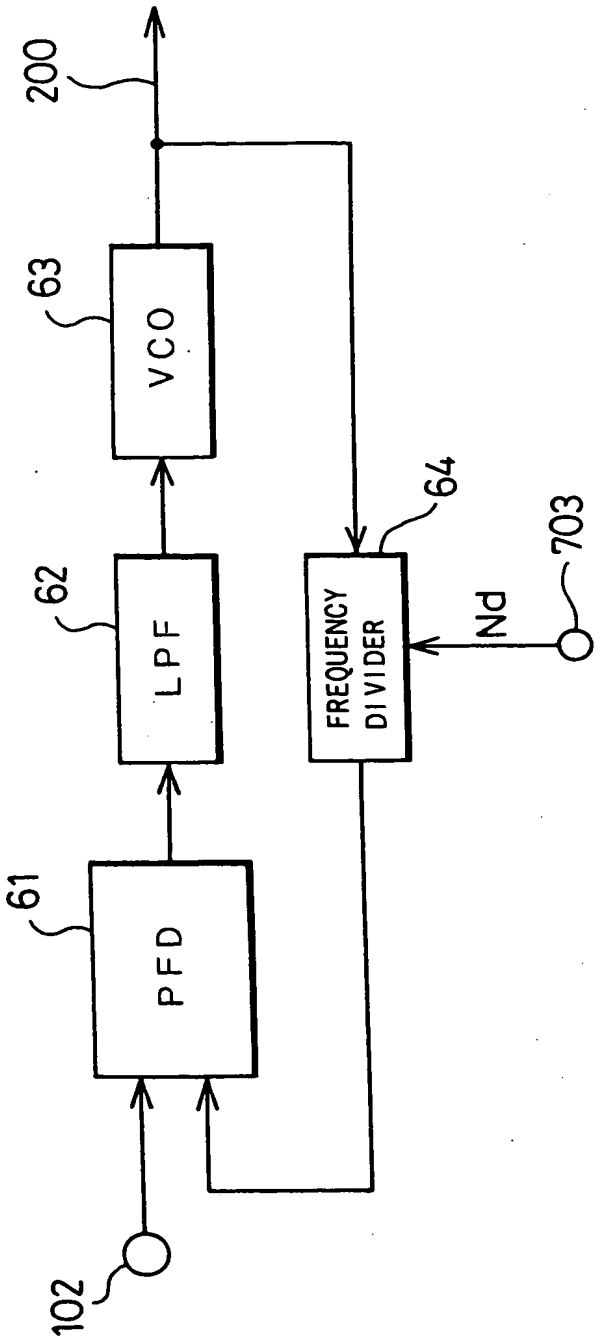



Fig. 2

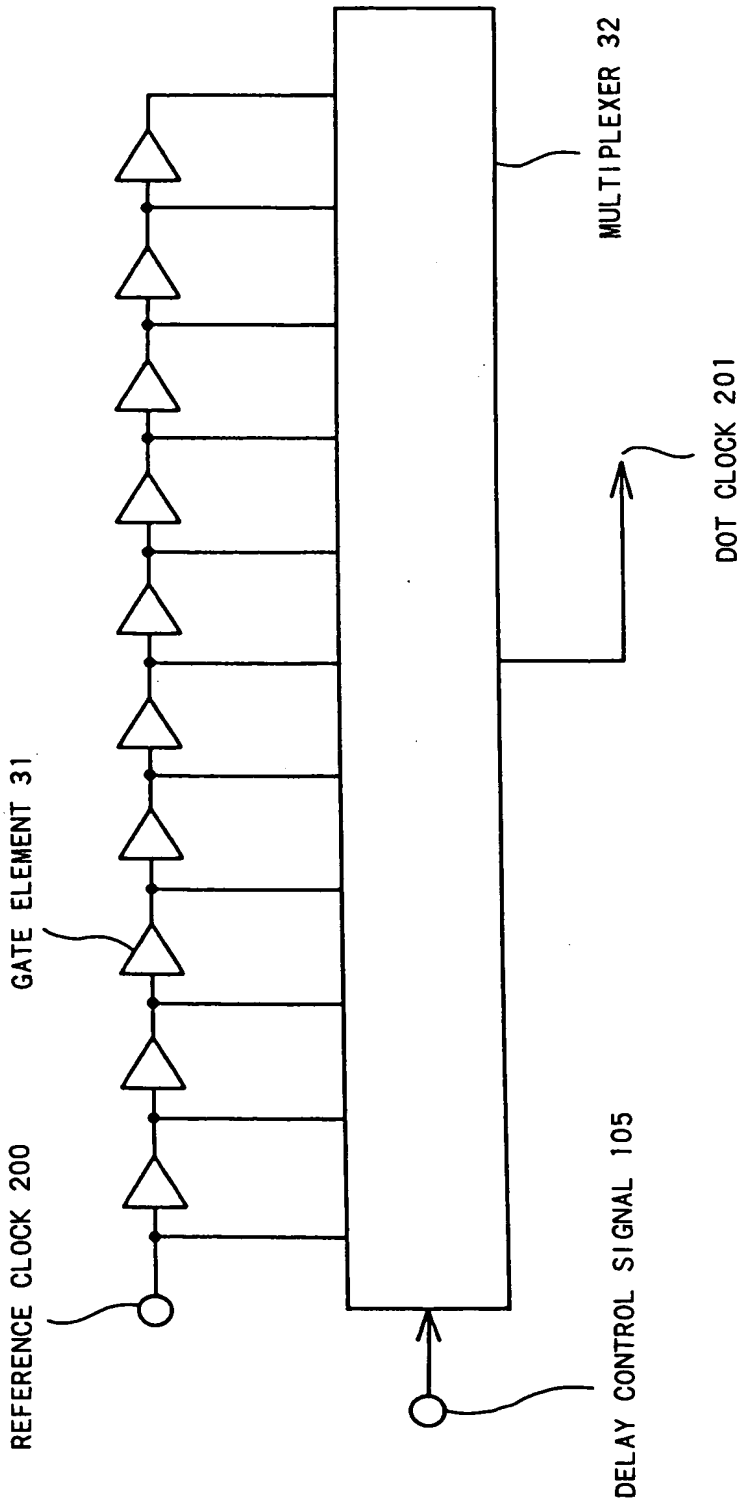

MULTIPLEXER 32
DOT CLOCK 201
GATE ELEMENT 31
REFERENCE CLOCK 200
DELAY CONTROL SIGNAL 105

Fig. 3

Fig. 4

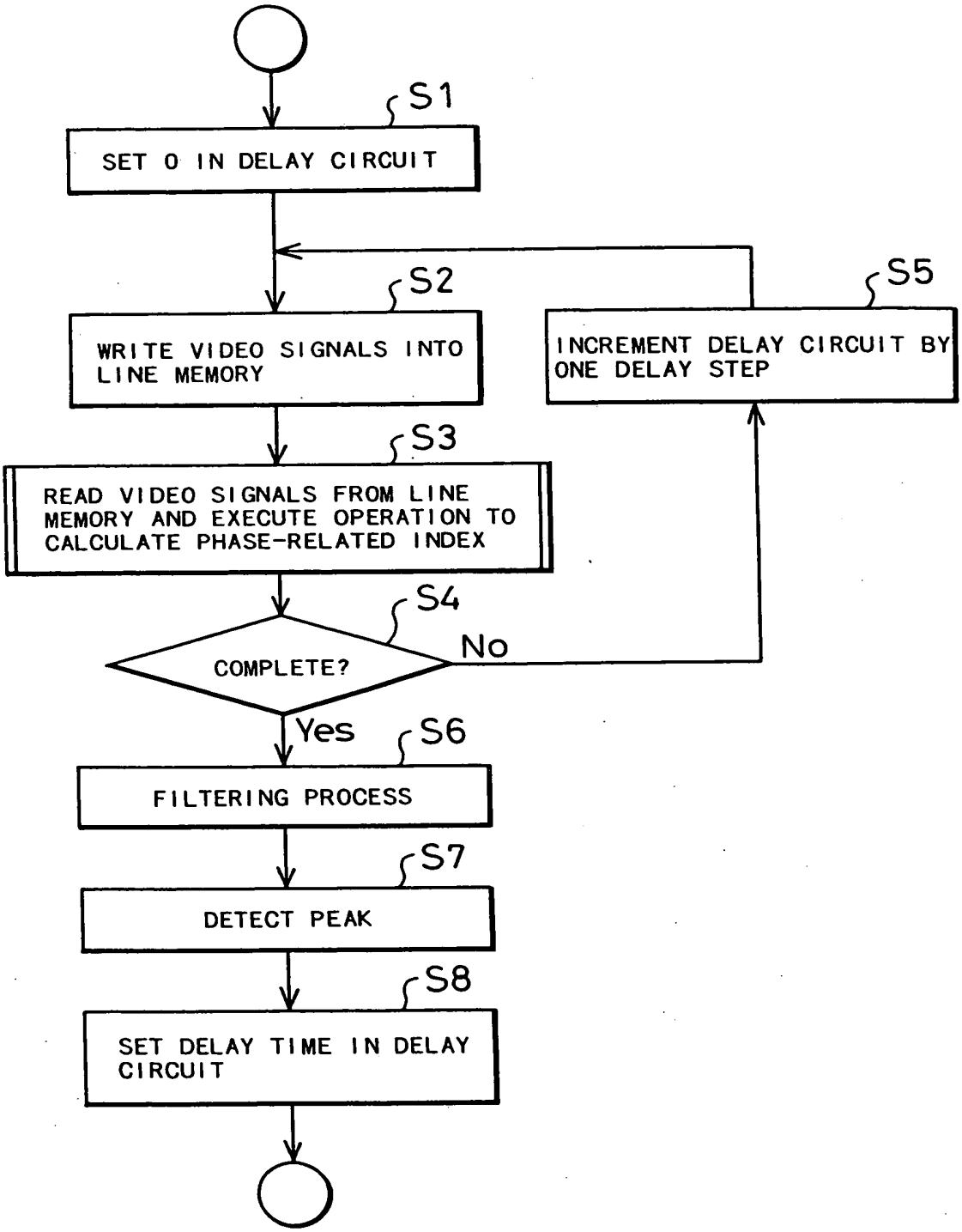

S1
SET 0 IN DELAY CIRCUIT
S2
WRITE VIDEO SIGNALS INTO LINE MEMORY
S3
READ VIDEO SIGNALS FROM LINE MEMORY AND EXECUTE OPERATION TO CALCULATE PHASE-RELATED INDEX
S4
COMPLETE?
No
Yes
S5
INCREMENT DELAY CIRCUIT BY ONE DELAY STEP
S6
FILTERING PROCESS
S7
DETECT PEAK
S8
SET DELAY TIME IN DELAY CIRCUIT

Fig. 5

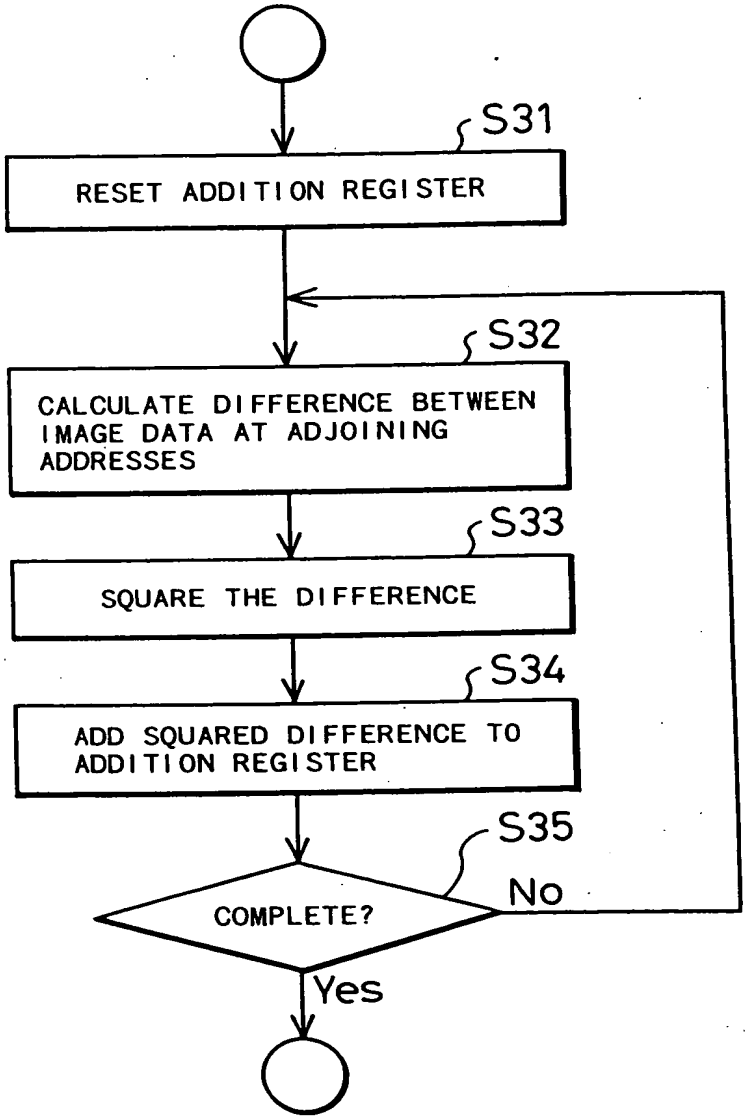

S31
RESET ADDITION REGISTER
S32
CALCULATE DIFFERENCE BETWEEN IMAGE DATA AT ADJOINING ADDRESSES
S33
SQUARE THE DIFFERENCE
S34
ADD SQUARED DIFFERENCE TO ADDITION REGISTER
S35
COMPLETE?
No
Yes

Fig. 6

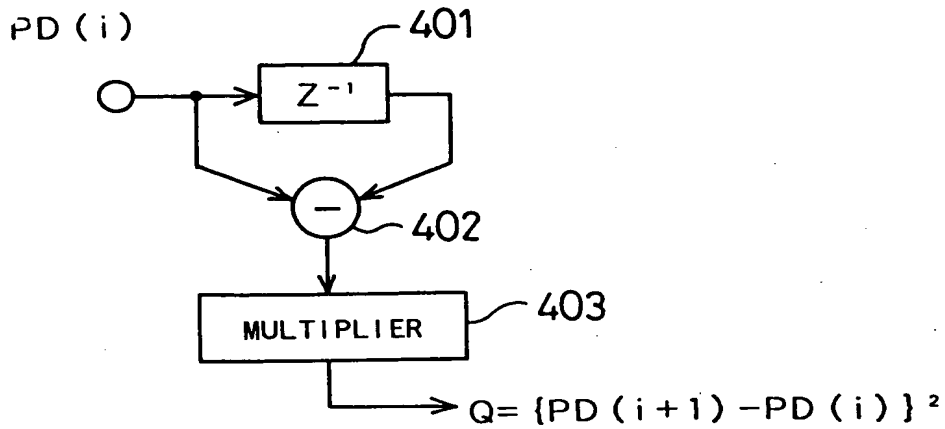
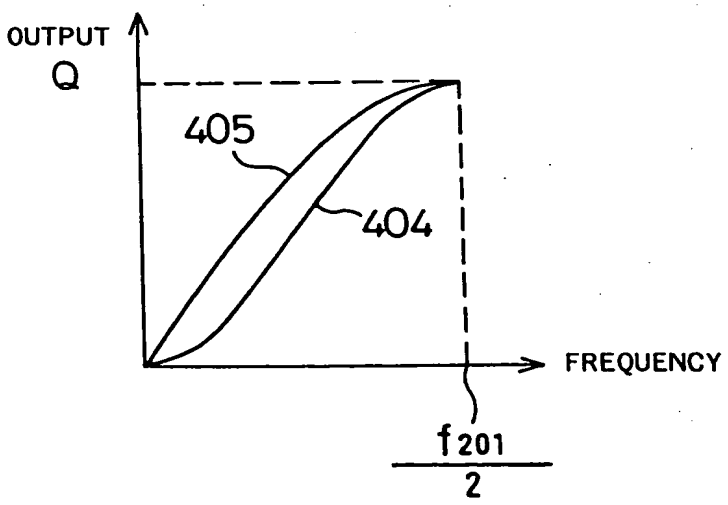

PD(i)
401
Z⁻¹
402
MULTIPLIER
403
Q={PD(i+1)−PD(i)}²

Fig. 7


OUTPUT
Q
405
404
FREQUENCY
f201
2

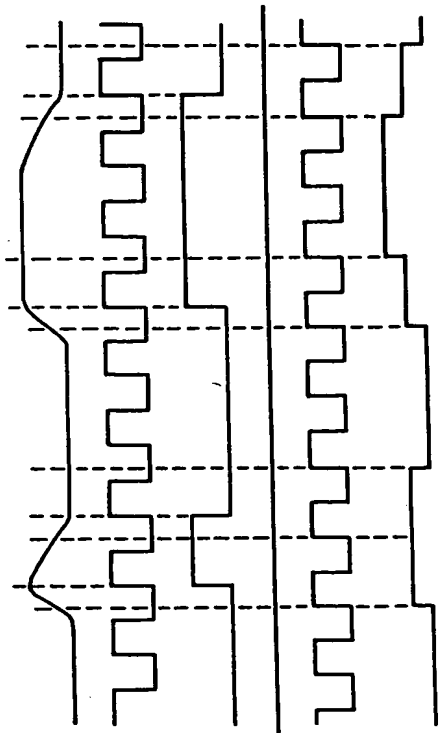


Fig. 8(a) VIDEO SIGNAL 101

Fig. 8(b) DOT CLOCK 201a

Fig. 8(c) A-D CONVERTER OUTPUT 110a

Fig. 8(d) DOT CLOCK 201b

Fig. 8(e) A-D CONVERTER OUTPUT 110b

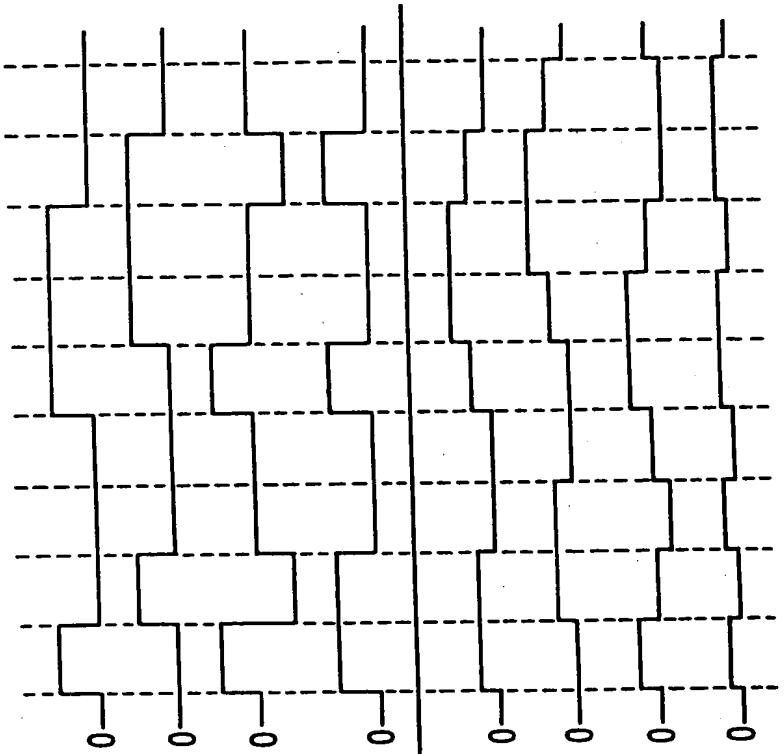



Fig. 9(a) LINE MEMORY OUTPUT 110a

Fig. 9(b) DELAY BY ONE CLOCK 221a

Fig. 9(c) DIFFERENCE 222a

Fig. 9(d) SQUARE 223a

Fig. 9(e) LINE MEMORY OUTPUT 110b

Fig. 9(f) DELAY BY ONE CLOCK 221b

Fig. 9(g) DIFFERENCE 222b

Fig. 9(h) SQUARE 223b

Fig. 10

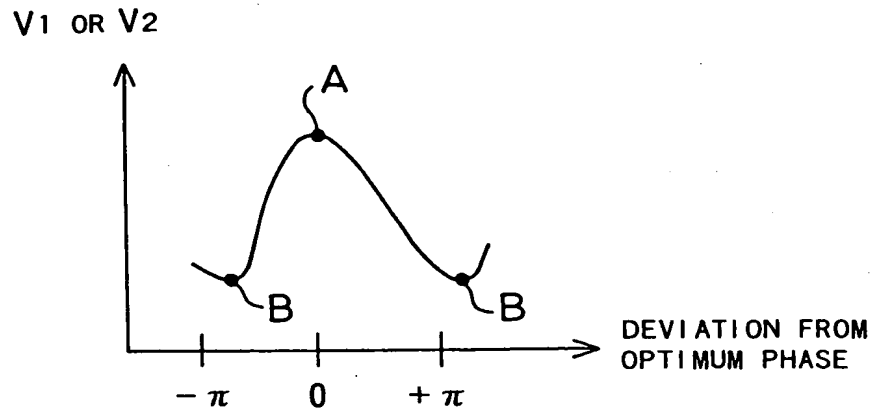


Fig. 11(A)

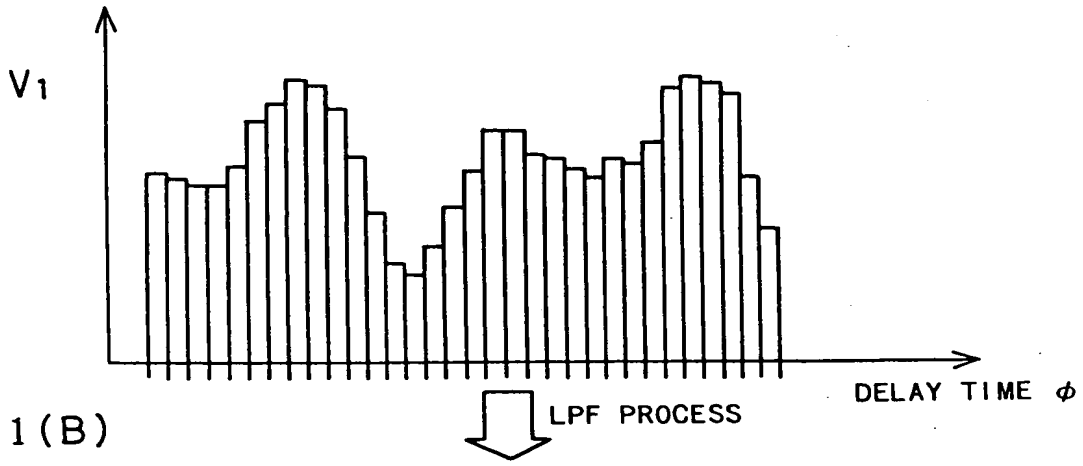
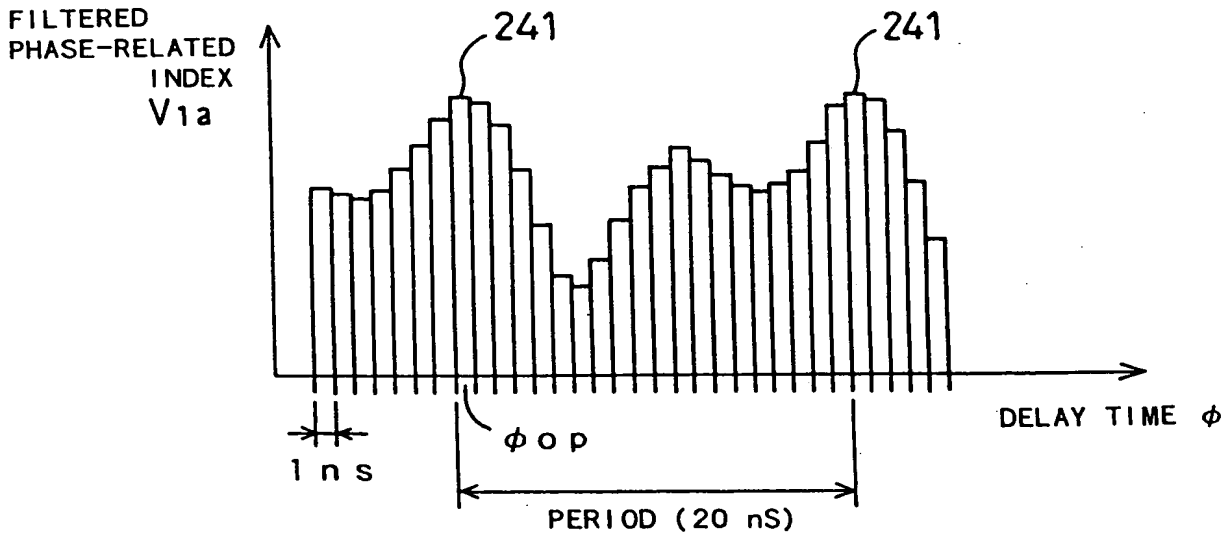



Fig. 11(B)



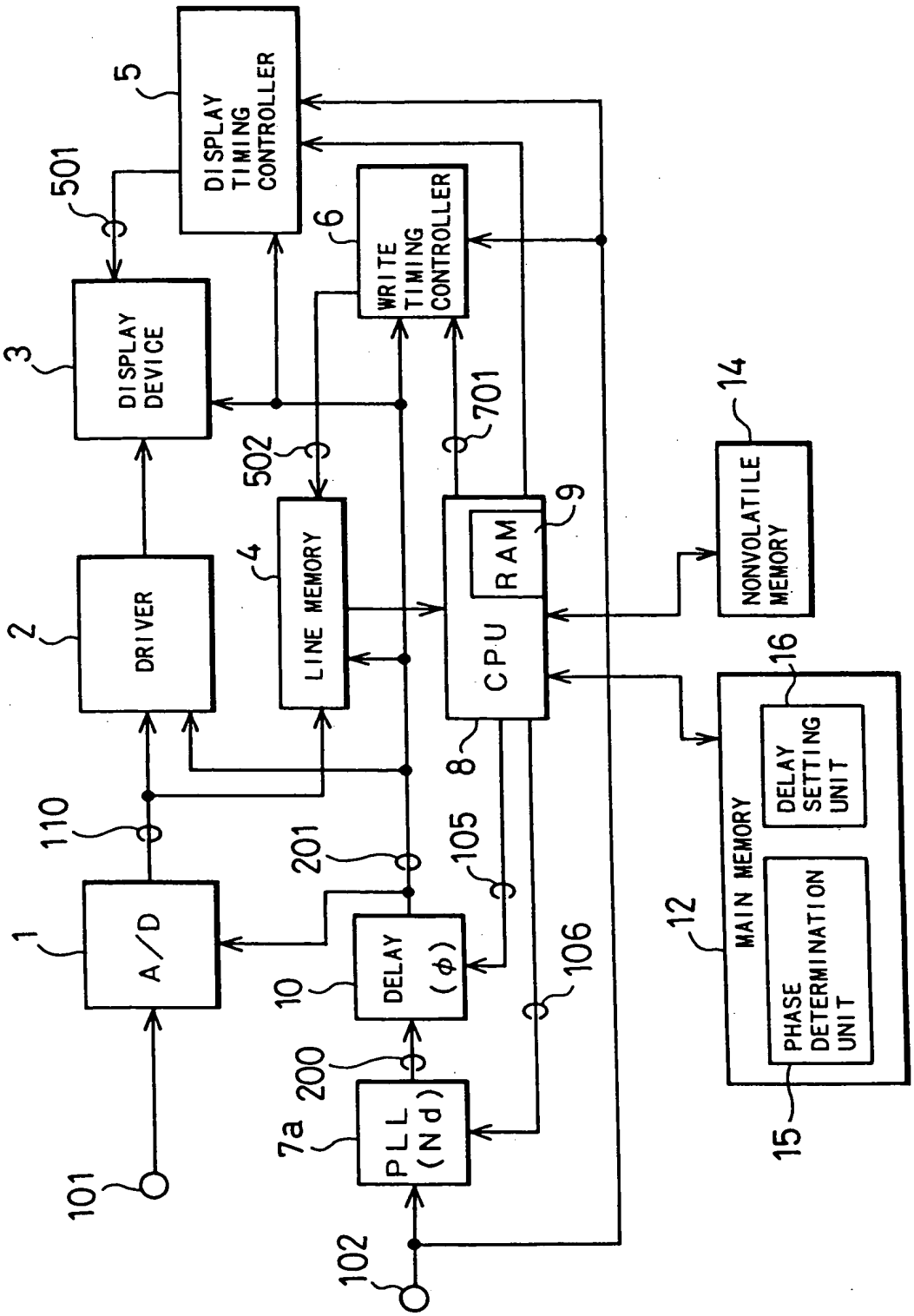

DISPLAY TIMING CONTROLLER
5
501
WRITE TIMING CONTROLLER
6
DISPLAY DEVICE
3
701
502
14
NONVOLATILE MEMORY
LINE MEMORY
4
RAM
9
DRIVER
2
CPU
8
16
DELAY SETTING UNIT
110
201
105
MAIN MEMORY
12
A/D
1
DELAY (φ)
10
106
PHASE DETERMINATION UNIT
15
200
7a
PLL (Nd)
101
102

Fig. 12

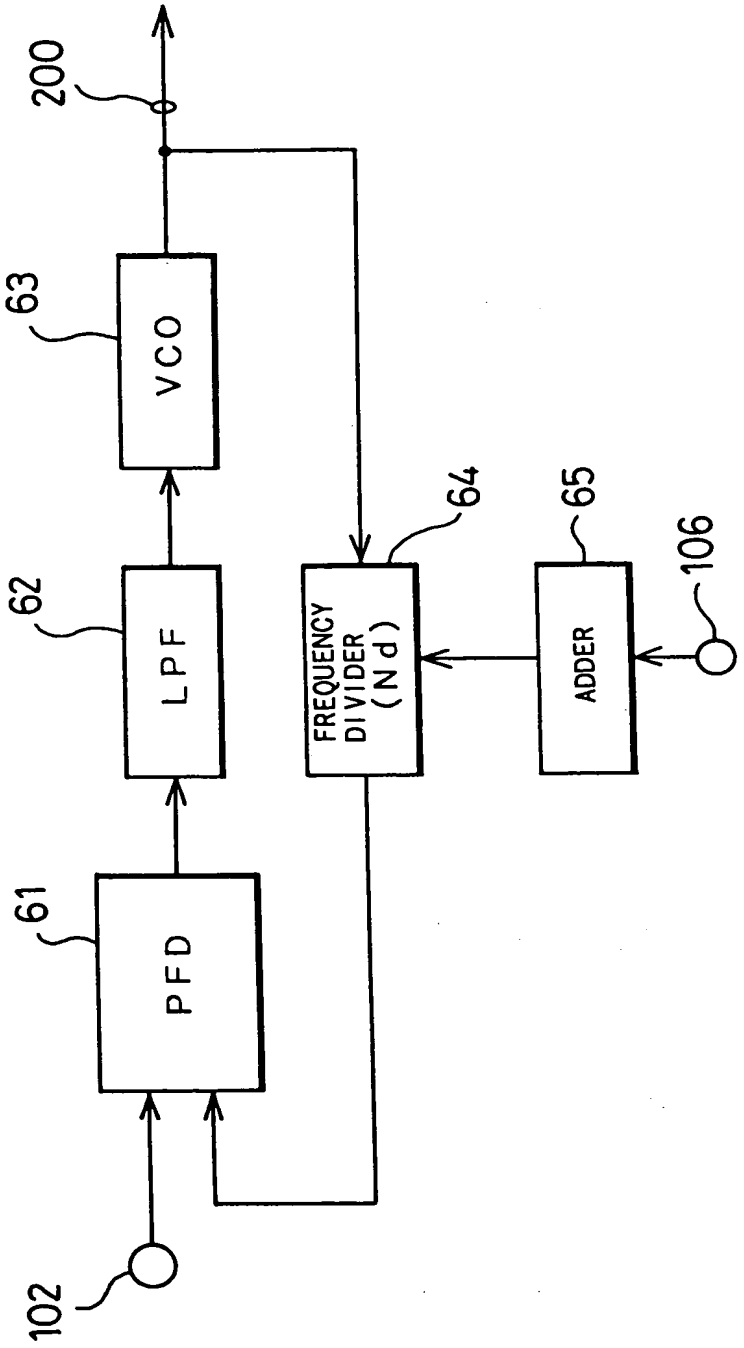

200
63
VCO
62
LPF
64
FREQUENCY DIVIDER (Nd)
65
ADDER
106
61
PFD
102

Fig. 13

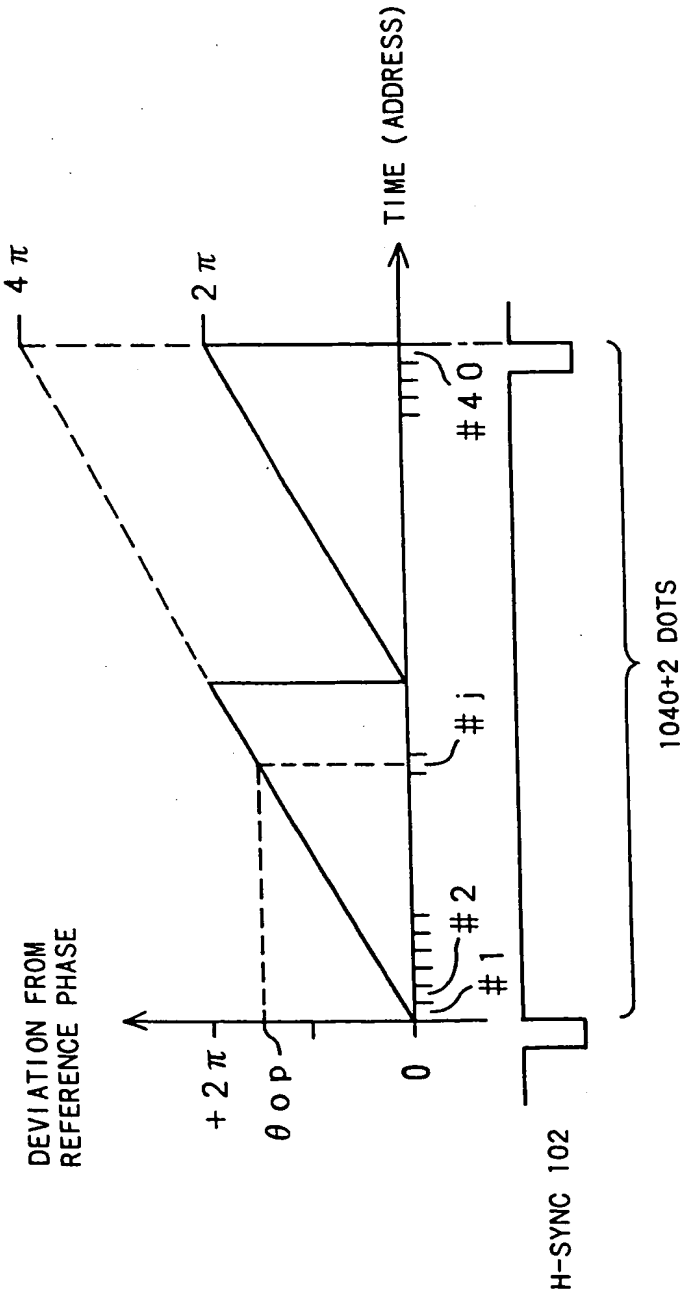

TIME (ADDRESS)
4 π
2 π
#40
#j
#2
#1
1040+2 DOTS
H-SYNC 102
DEVIATION FROM REFERENCE PHASE
+2 π
θ o p
0

Fig. 14

Fig. 15

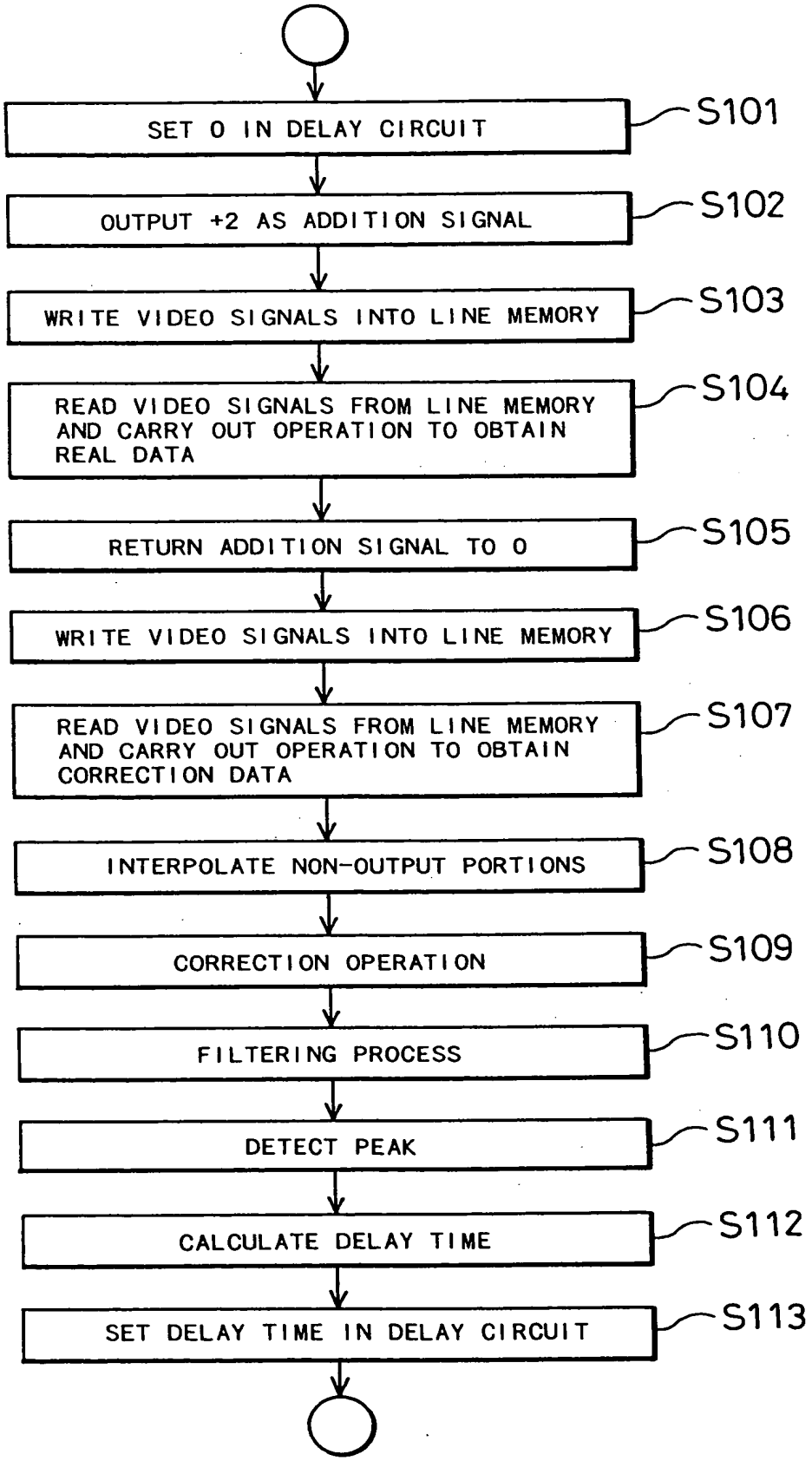

SET 0 IN DELAY CIRCUIT
S101
OUTPUT +2 AS ADDITION SIGNAL
S102
WRITE VIDEO SIGNALS INTO LINE MEMORY
S103
READ VIDEO SIGNALS FROM LINE MEMORY AND CARRY OUT OPERATION TO OBTAIN REAL DATA
S104
RETURN ADDITION SIGNAL TO 0
S105
WRITE VIDEO SIGNALS INTO LINE MEMORY
S106
READ VIDEO SIGNALS FROM LINE MEMORY AND CARRY OUT OPERATION TO OBTAIN CORRECTION DATA
S107
INTERPOLATE NON-OUTPUT PORTIONS
S108
CORRECTION OPERATION
S109
FILTERING PROCESS
S110
DETECT PEAK
S111
CALCULATE DELAY TIME
S112
SET DELAY TIME IN DELAY CIRCUIT
S113

Fig. 16(A)

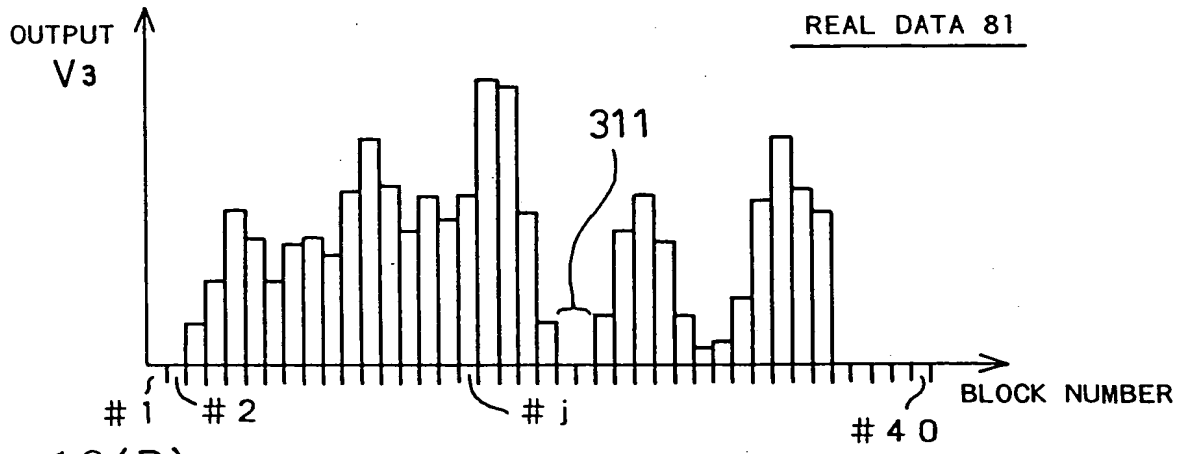



Fig. 16(B)

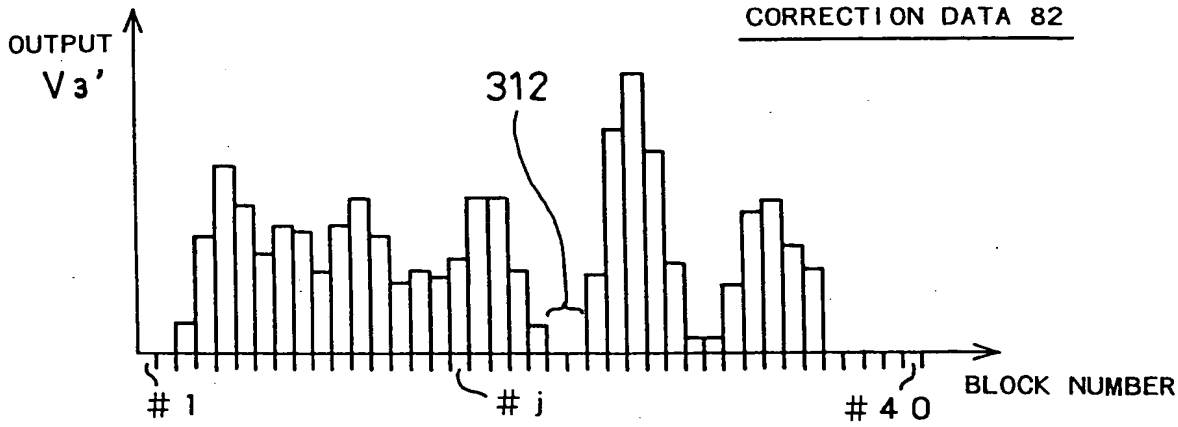
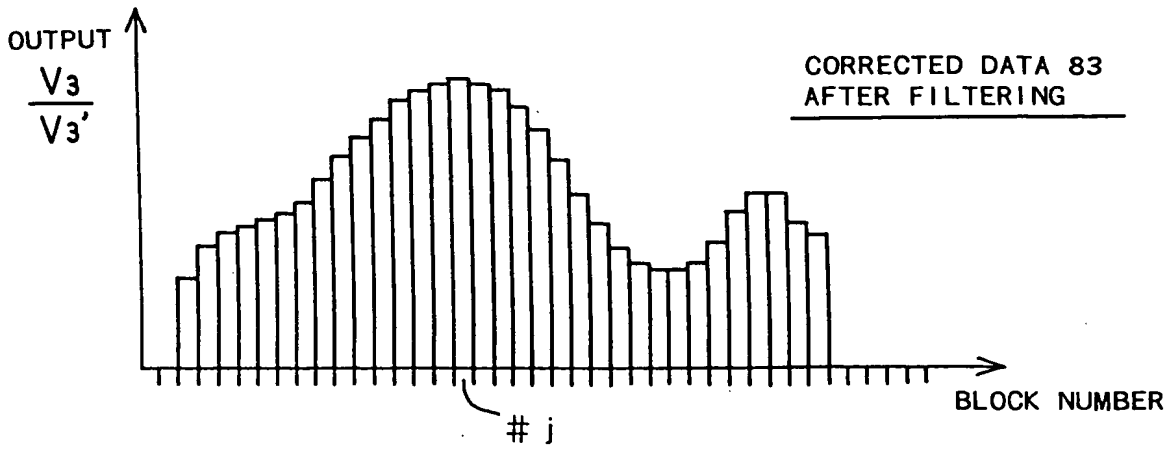



Fig. 16(C)



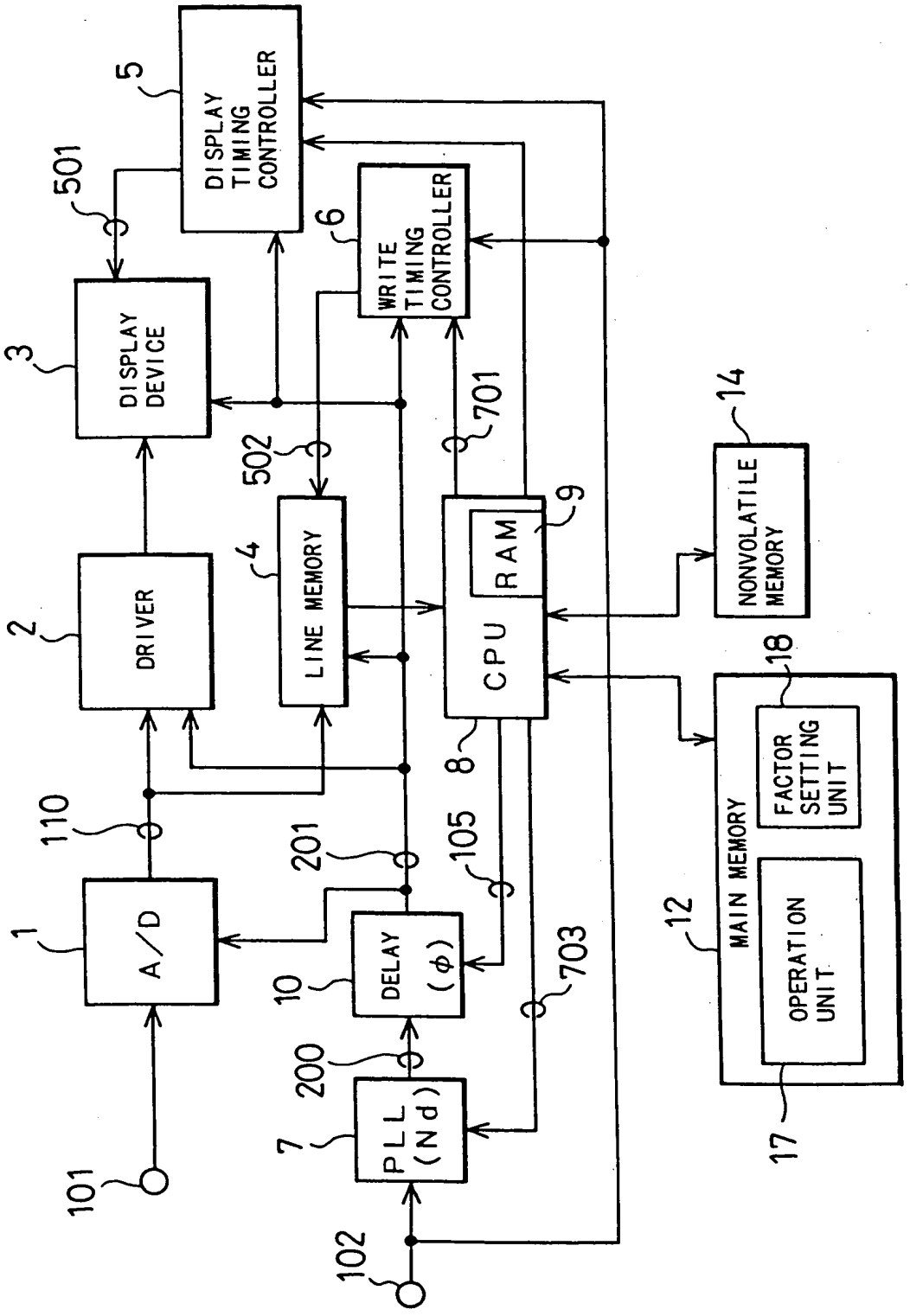

DISPLAY TIMING CONTROLLER
5
501
WRITE TIMING CONTROLLER
6
DISPLAY DEVICE
3
701
502
14
NONVOLATILE MEMORY
LINE MEMORY
4
RAM
9
DRIVER
2
CPU
8
18
FACTOR SETTING UNIT
110
201
105
MAIN MEMORY
12
A/D
1
DELAY (φ)
10
703
OPERATION UNIT
200
PLL (Nd)
7
17
101
102

Fig. 17

Fig. 18(a) H-SYNC 102

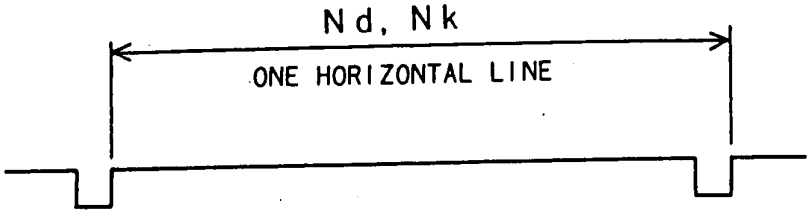
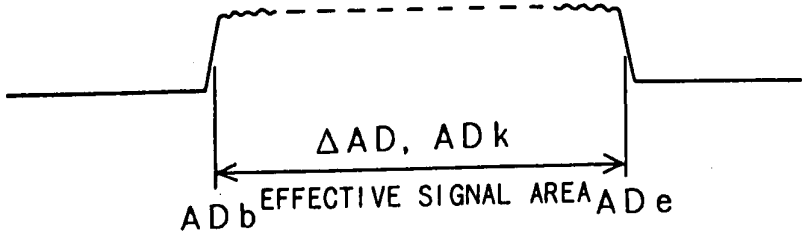


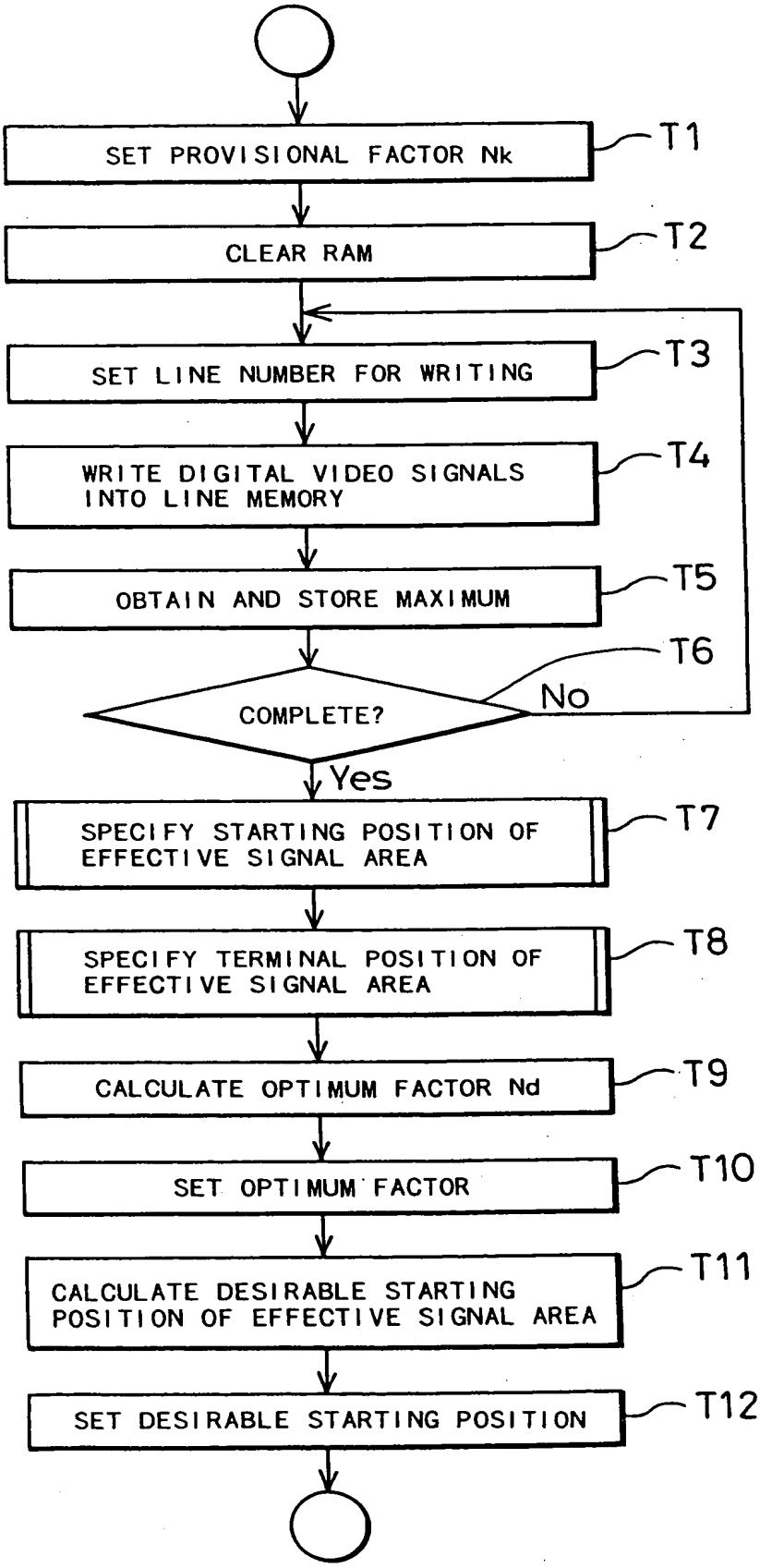

Fig. 18(b) VIDEO SIGNAL 101




$$\frac{Nd}{Nk} = \frac{\Delta AD}{\Delta ADk}$$

$$Nd = \frac{\Delta AD}{\Delta ADk} \times Nk$$

Fig. 19


SET PROVISIONAL FACTOR Nk
T1
CLEAR RAM
T2
SET LINE NUMBER FOR WRITING
T3
WRITE DIGITAL VIDEO SIGNALS INTO LINE MEMORY
T4
OBTAIN AND STORE MAXIMUM
T5
COMPLETE?
T6
No
Yes
SPECIFY STARTING POSITION OF EFFECTIVE SIGNAL AREA
T7
SPECIFY TERMINAL POSITION OF EFFECTIVE SIGNAL AREA
T8
CALCULATE OPTIMUM FACTOR Nd
T9
SET OPTIMUM FACTOR
T10
CALCULATE DESIRABLE STARTING POSITION OF EFFECTIVE SIGNAL AREA
T11
SET DESIRABLE STARTING POSITION
T12

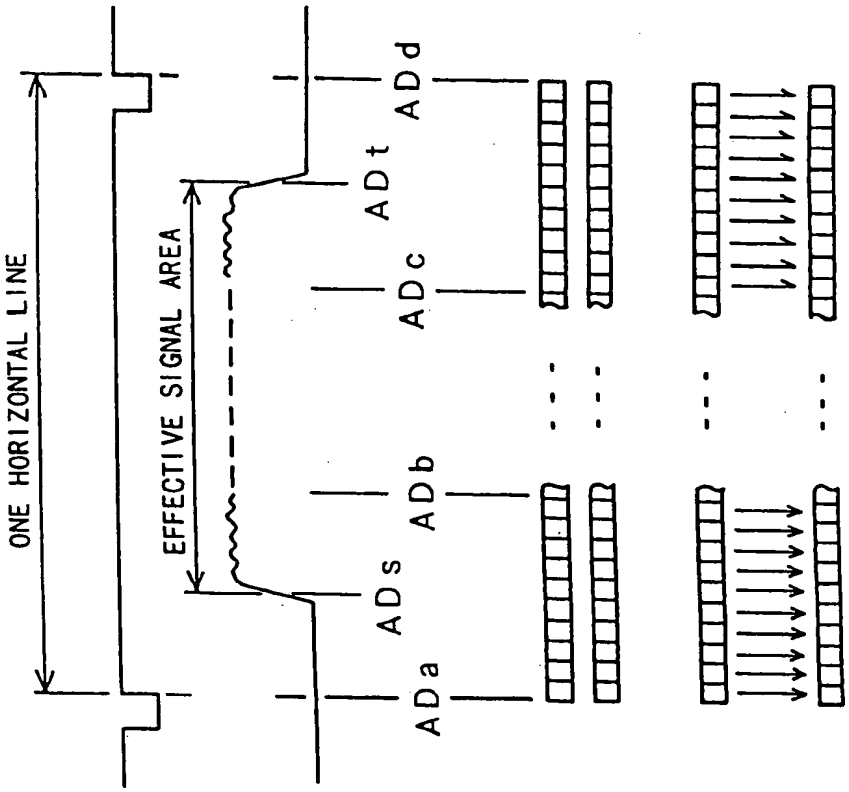



FIG. 20A
H-SYNC 102

FIG. 20B
VIDEO SIGNAL 101

FIG. 20C
IMAGE DATA FOR PLURAL LINES

FIG. 20D
MAXIMUM VALUES

Fig. 21

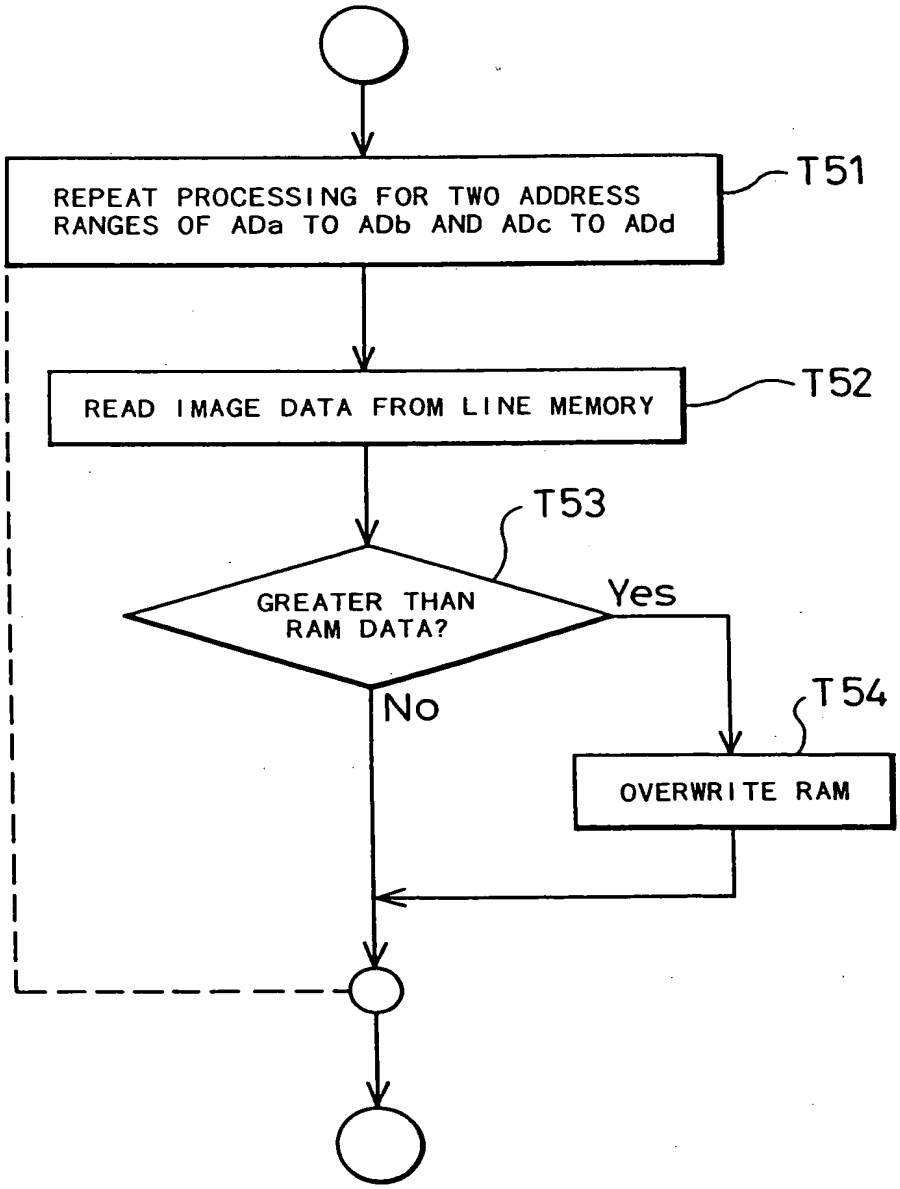

REPEAT PROCESSING FOR TWO ADDRESS RANGES OF ADa TO ADb AND ADc TO ADd
T51
READ IMAGE DATA FROM LINE MEMORY
T52
T53
GREATER THAN RAM DATA?
Yes
No
T54
OVERWRITE RAM

Fig. 22

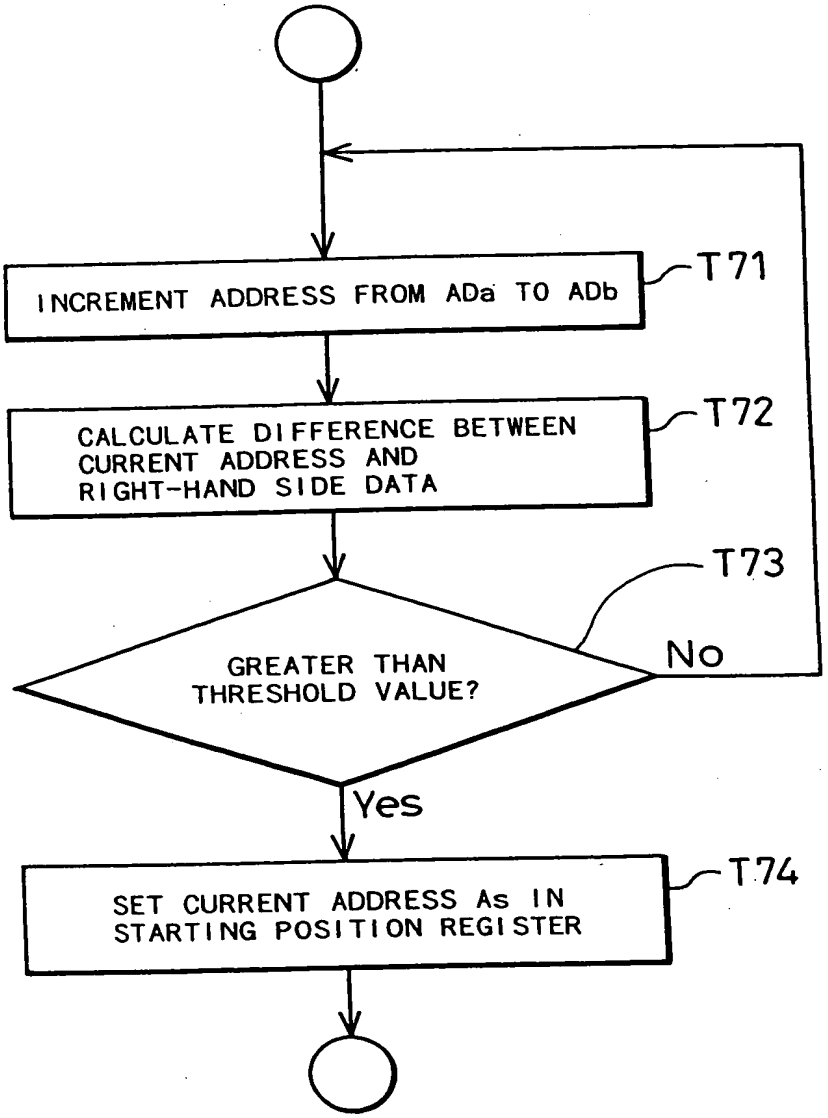

INCREMENT ADDRESS FROM ADa TO ADb
T71
CALCULATE DIFFERENCE BETWEEN CURRENT ADDRESS AND RIGHT-HAND SIDE DATA
T72
T73
GREATER THAN THRESHOLD VALUE?
No
Yes
SET CURRENT ADDRESS As IN STARTING POSITION REGISTER
T74

Fig. 23

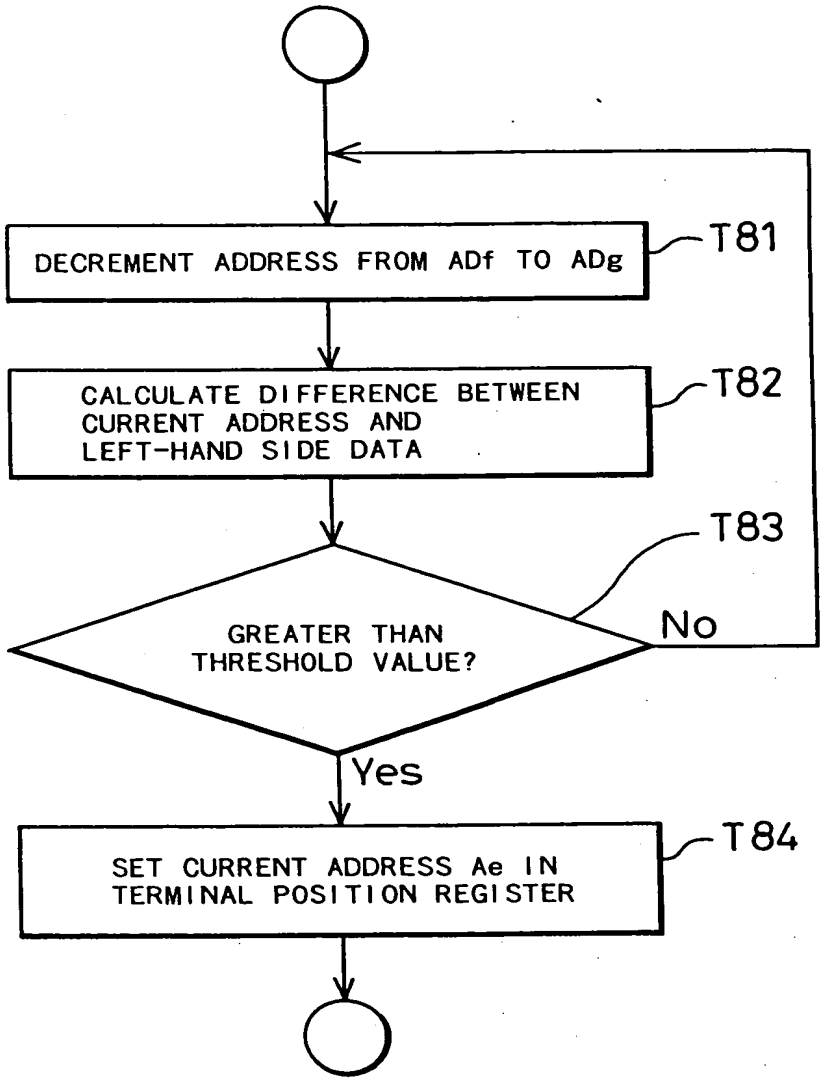
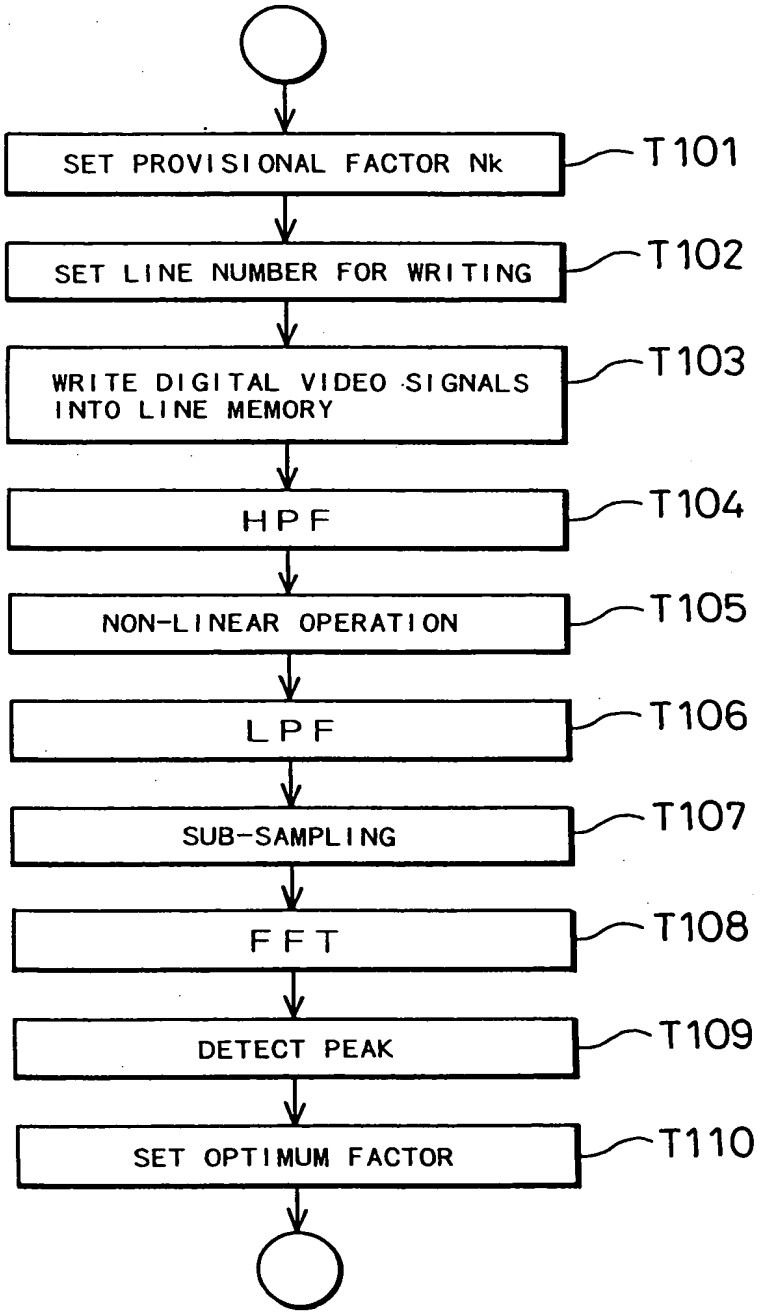

DECREMENT ADDRESS FROM ADf TO ADg
T81
CALCULATE DIFFERENCE BETWEEN CURRENT ADDRESS AND LEFT-HAND SIDE DATA
T82
T83
GREATER THAN THRESHOLD VALUE?
No
Yes
SET CURRENT ADDRESS Ae IN TERMINAL POSITION REGISTER
T84

Fig. 24


SET PROVISIONAL FACTOR Nk
T101
SET LINE NUMBER FOR WRITING
T102
WRITE DIGITAL VIDEO SIGNALS INTO LINE MEMORY
T103
HPF
T104
NON-LINEAR OPERATION
T105
LPF
T106
SUB-SAMPLING
T107
FFT
T108
DETECT PEAK
T109
SET OPTIMUM FACTOR
T110

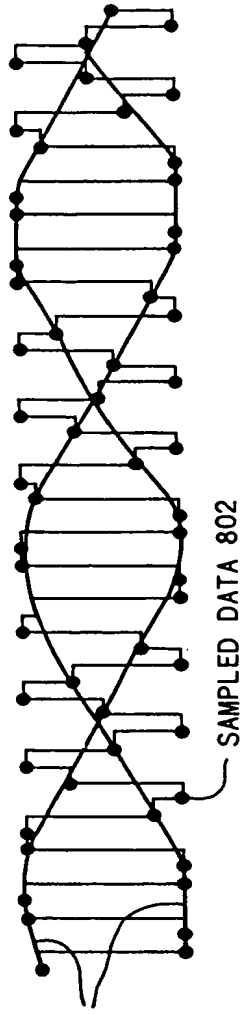



Fig. 25(a)

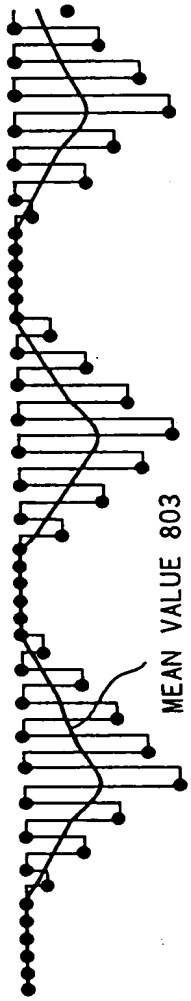



Fig. 25(b)

Fig. 26(a)

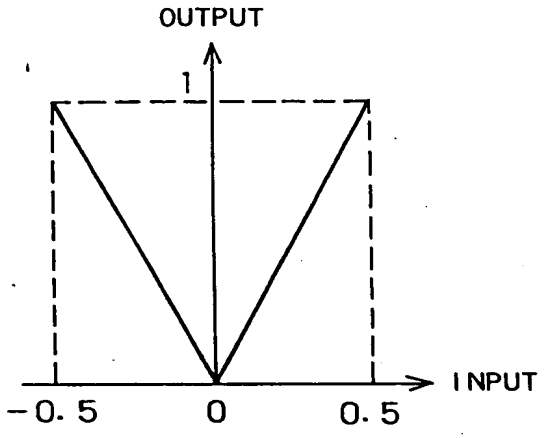



Fig. 26(b)

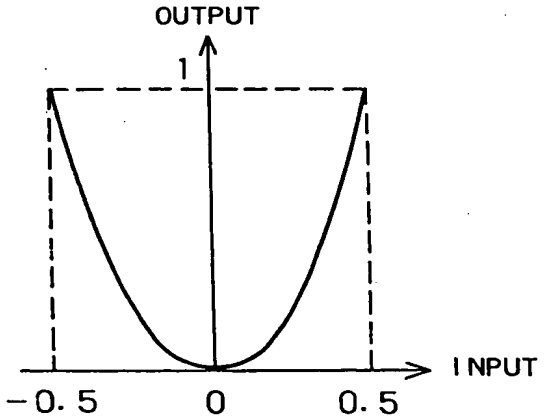


Fig. 27

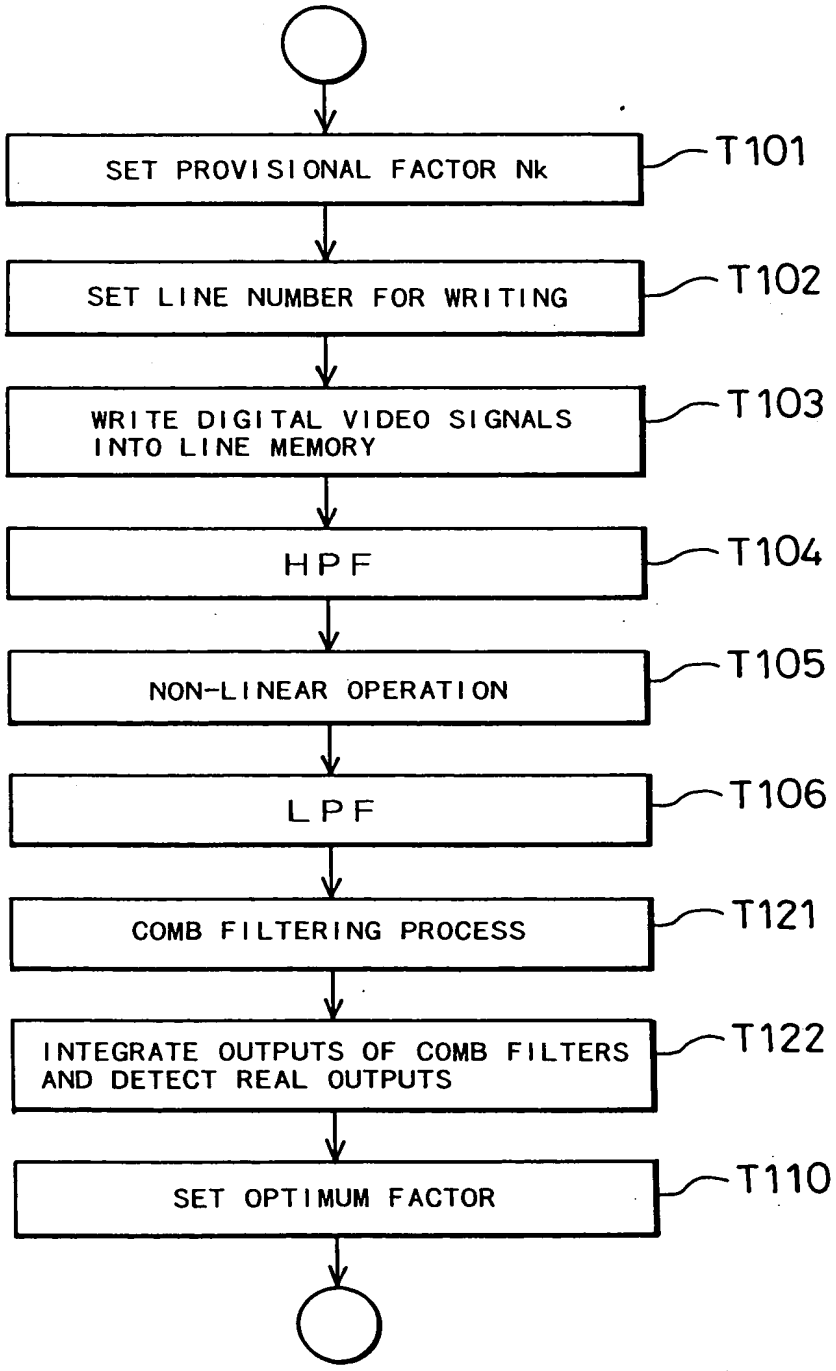

SET PROVISIONAL FACTOR Nk
T101
SET LINE NUMBER FOR WRITING
T102
WRITE DIGITAL VIDEO SIGNALS INTO LINE MEMORY
T103
HPF
T104
NON-LINEAR OPERATION
T105
LPF
T106
COMB FILTERING PROCESS
T121
INTEGRATE OUTPUTS OF COMB FILTERS AND DETECT REAL OUTPUTS
T122
SET OPTIMUM FACTOR
T110

Fig. 28

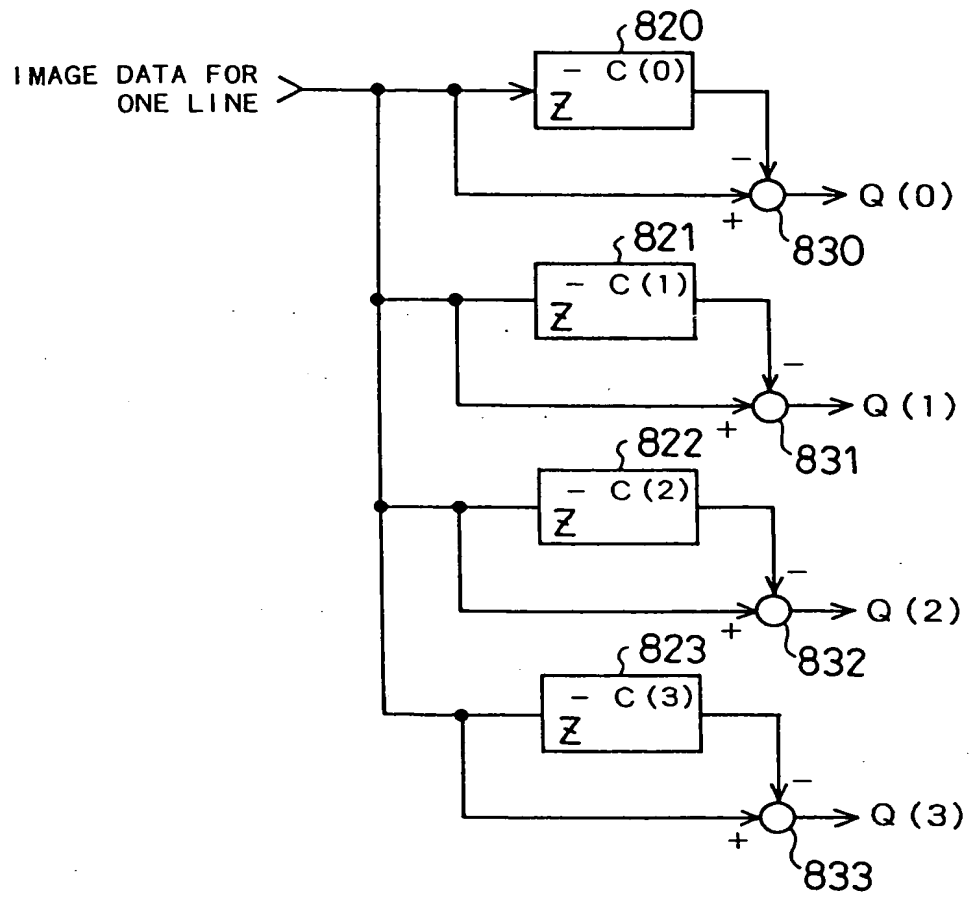


IMAGE DATA FOR ONE LINE
820
C (0)
Z
Q (0)
830
821
C (1)
Z
Q (1)
831
822
C (2)
Z
Q (2)
832
823
C (3)
Z
Q (3)
833

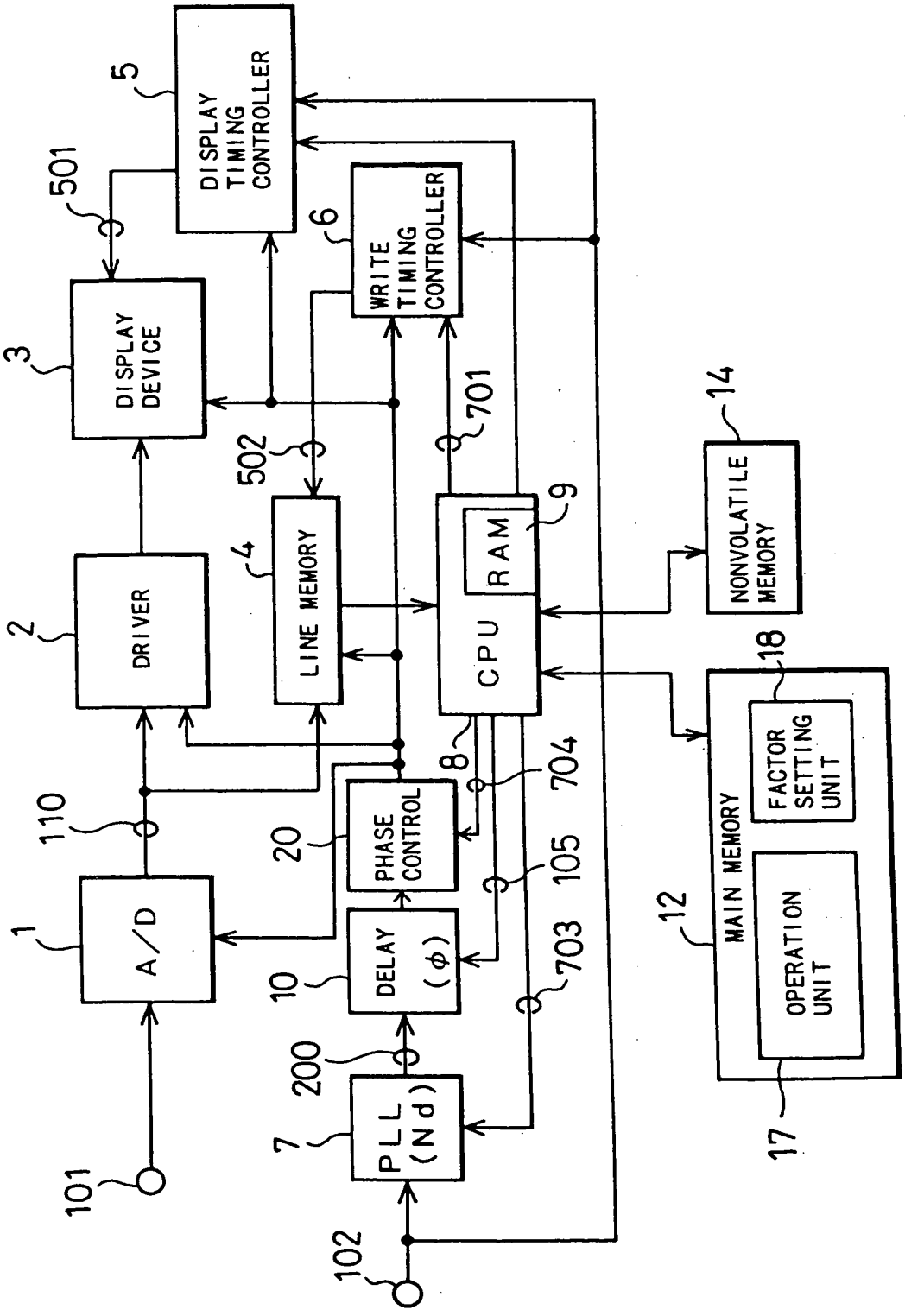

DISPLAY TIMING CONTROLLER
5
501
WRITE TIMING CONTROLLER
6
DISPLAY DEVICE
3
701
502
NONVOLATILE MEMORY
14
LINE MEMORY
4
RAM
9
DRIVER
2
CPU
8
704
18
FACTOR SETTING UNIT
110
PHASE CONTROL
20
105
MAIN MEMORY
12
A/D
1
DELAY (φ)
10
703
OPERATION UNIT
17
200
PLL (Nd)
7
101
102

Fig. 29

Fig. 30

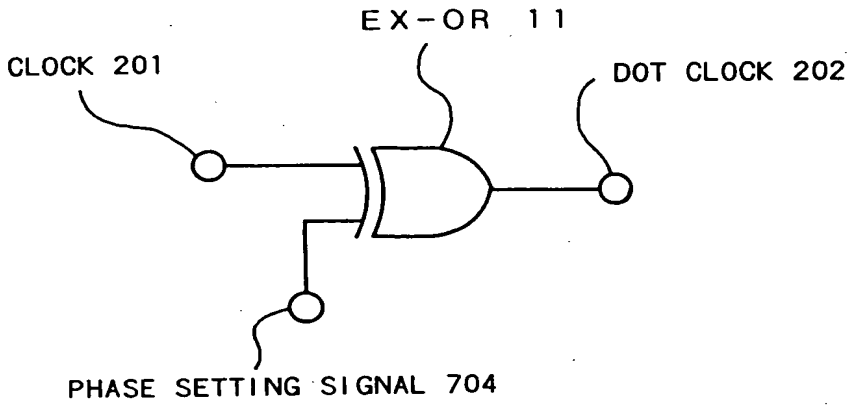


Fig. 31

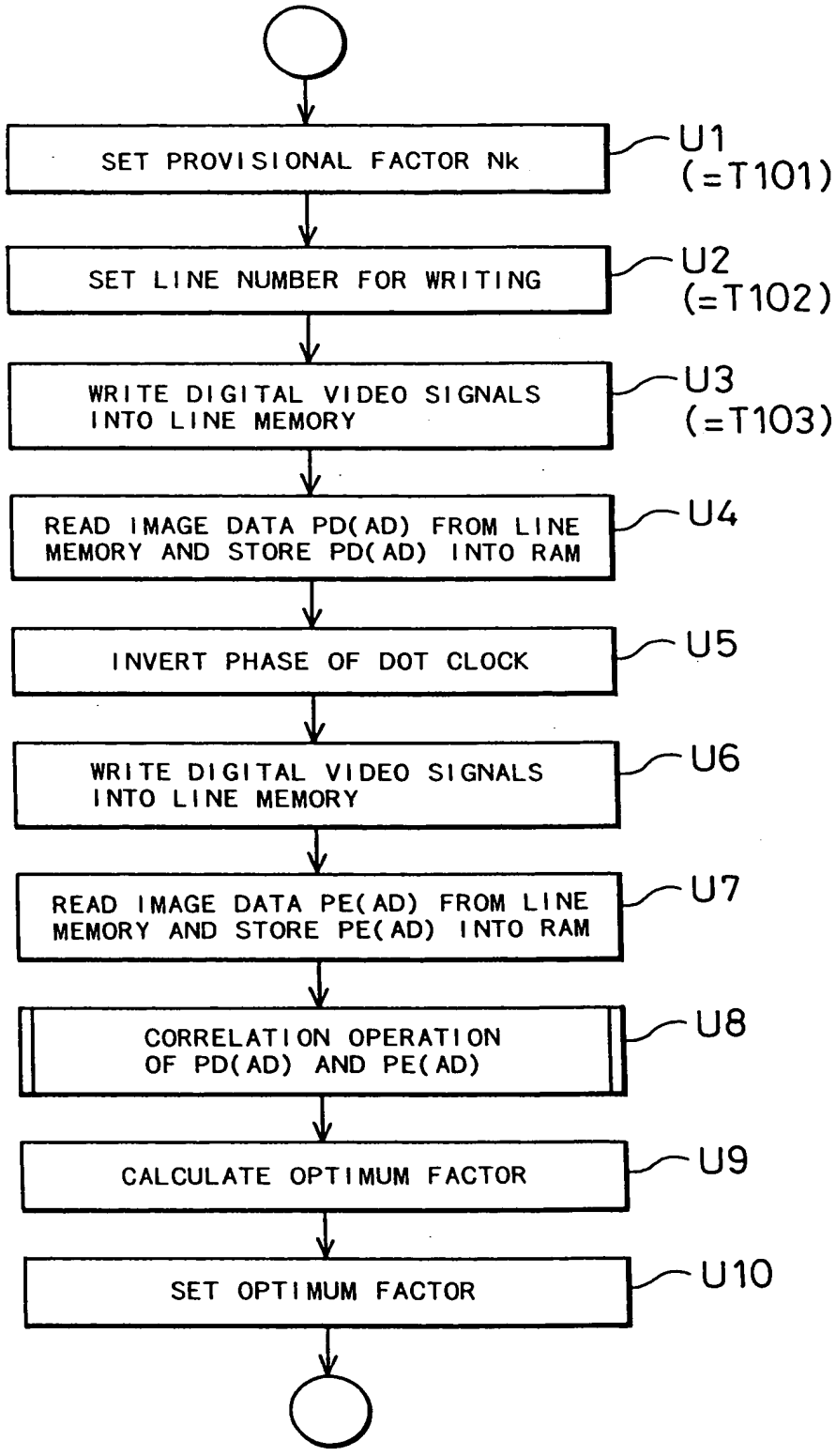

SET PROVISIONAL FACTOR Nk
U1 (=T101)
SET LINE NUMBER FOR WRITING
U2 (=T102)
WRITE DIGITAL VIDEO SIGNALS INTO LINE MEMORY
U3 (=T103)
READ IMAGE DATA PD(AD) FROM LINE MEMORY AND STORE PD(AD) INTO RAM
U4
INVERT PHASE OF DOT CLOCK
U5
WRITE DIGITAL VIDEO SIGNALS INTO LINE MEMORY
U6
READ IMAGE DATA PE(AD) FROM LINE MEMORY AND STORE PE(AD) INTO RAM
U7
CORRELATION OPERATION OF PD(AD) AND PE(AD)
U8
CALCULATE OPTIMUM FACTOR
U9
SET OPTIMUM FACTOR
U10

Fig. 32

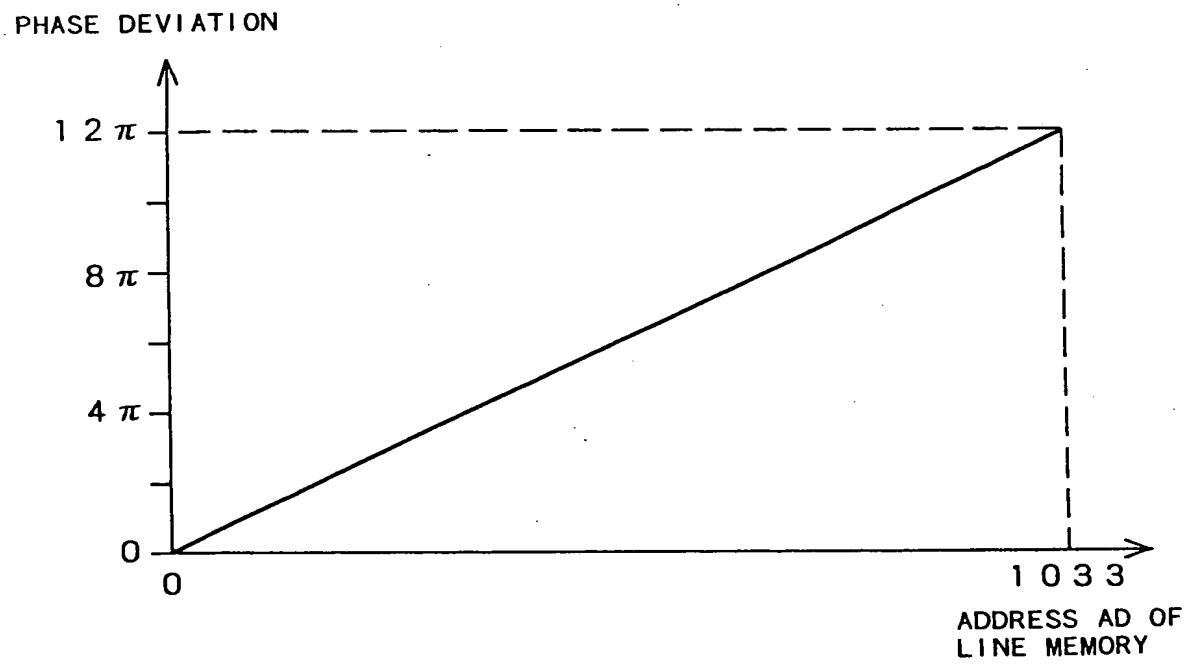


Fig. 33(a)

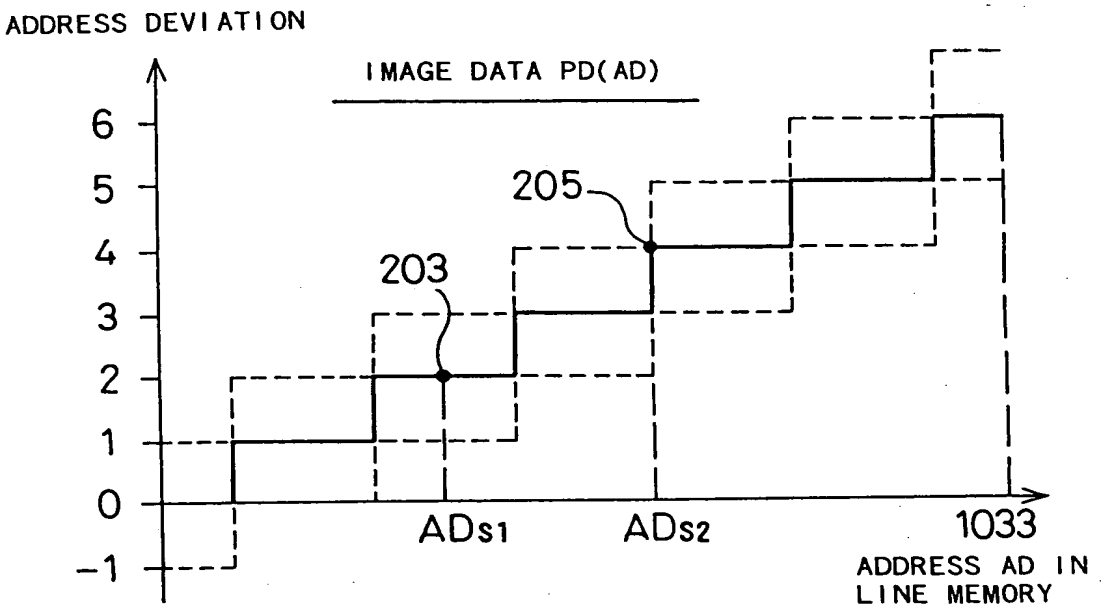



Fig. 33(b)

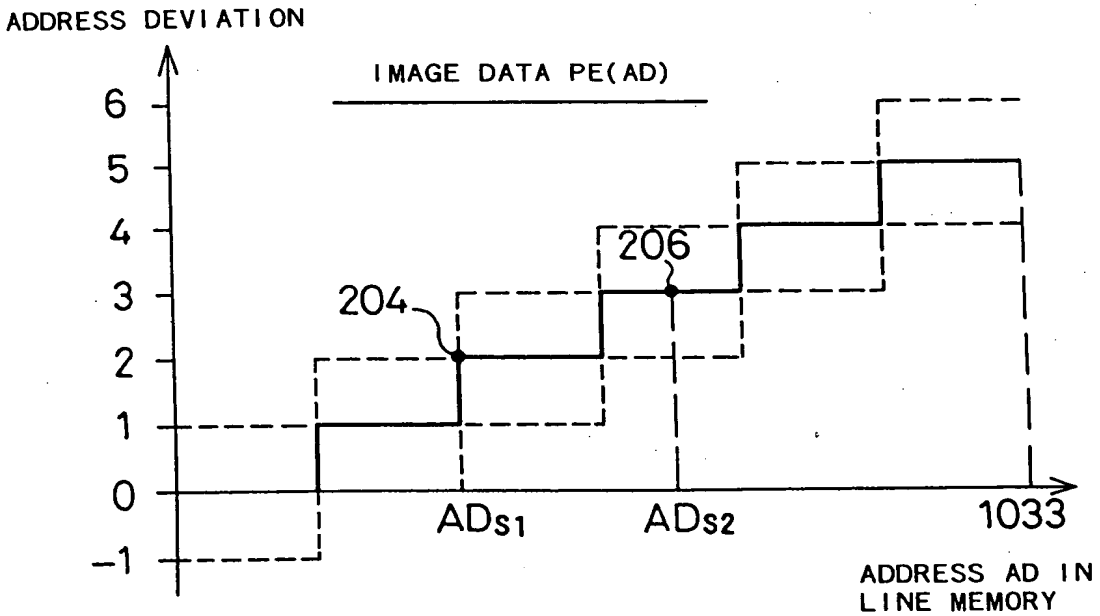


Fig. 34(a) PD (AD)

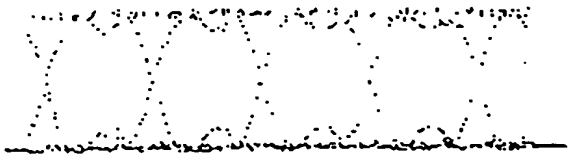


Fig. 34(b) PE (AD)

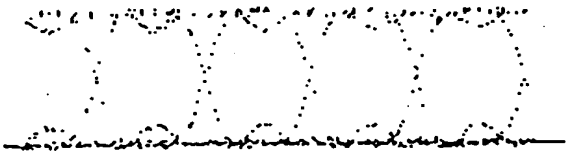


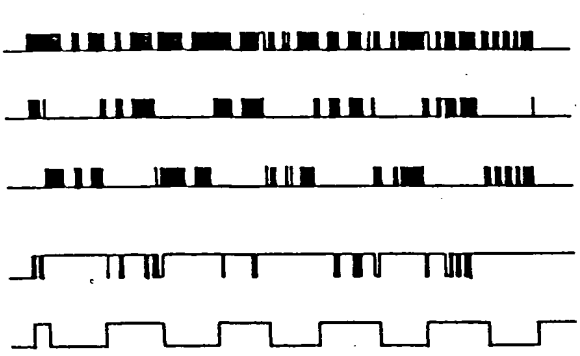
Fig. 34(c) A (AD)

Fig. 34(d) B (AD)

Fig. 34(e) C (AD)

Fig. 34(f) Q1 (AD)

Fig. 34(g) Q2 (AD)



VIDEO SIGNAL 101

Fig. 35(a)

Fig. 35(b)

Fig. 35(c)

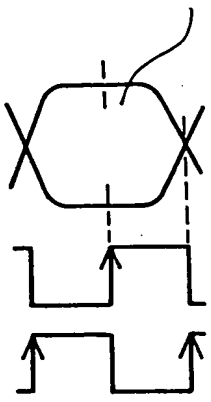
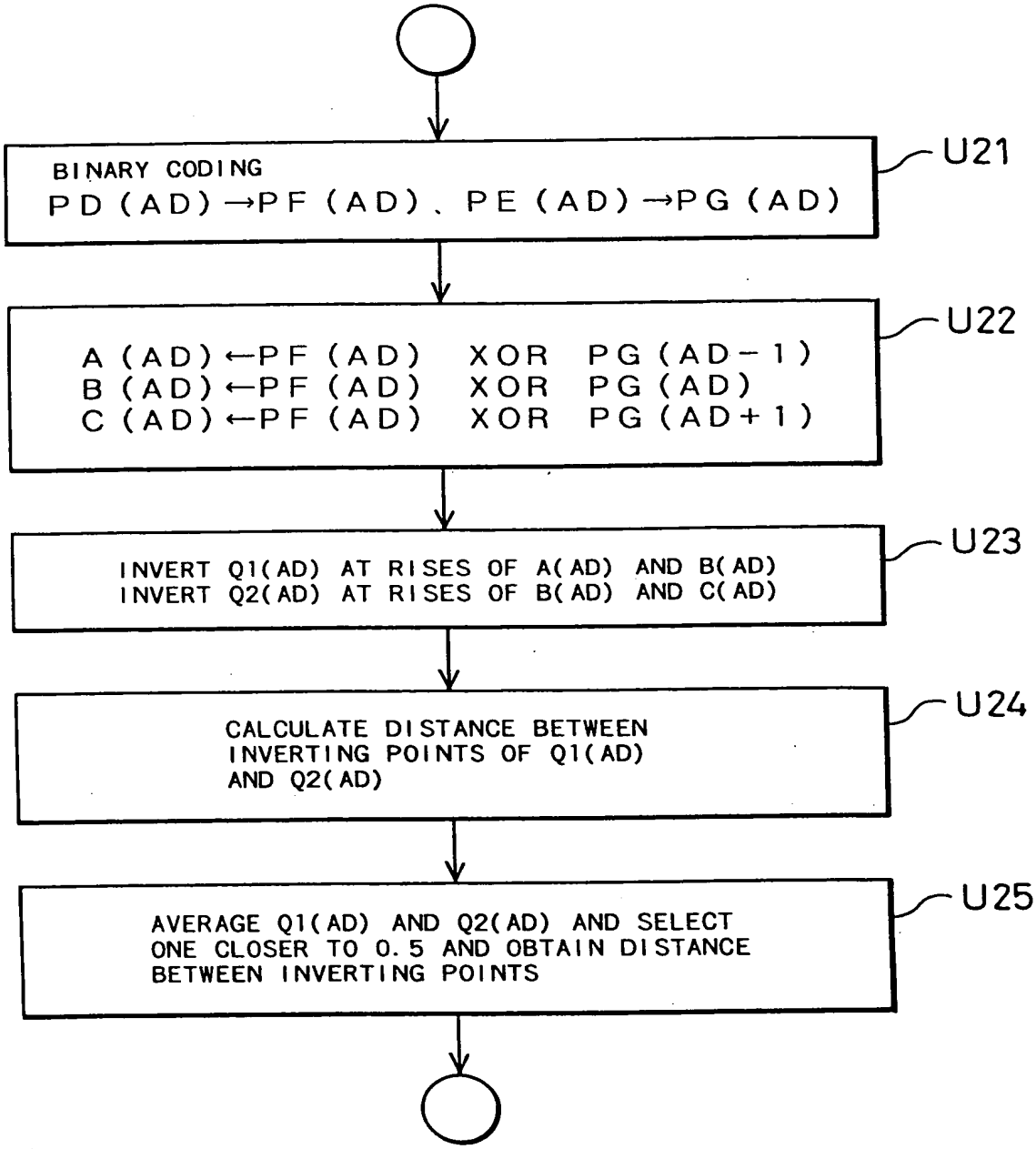


Fig. 36


BINARY CODING
PD(AD)→PF(AD)、PE(AD)→PG(AD)
U21
A(AD)←PF(AD) XOR PG(AD-1)
B(AD)←PF(AD) XOR PG(AD)
C(AD)←PF(AD) XOR PG(AD+1)
U22
INVERT Q1(AD) AT RISES OF A(AD) AND B(AD)
INVERT Q2(AD) AT RISES OF B(AD) AND C(AD)
U23
CALCULATE DISTANCE BETWEEN
INVERTING POINTS OF Q1(AD)
AND Q2(AD)
U24
AVERAGE Q1(AD) AND Q2(AD) AND SELECT
ONE CLOSER TO 0.5 AND OBTAIN DISTANCE
BETWEEN INVERTING POINTS
U25

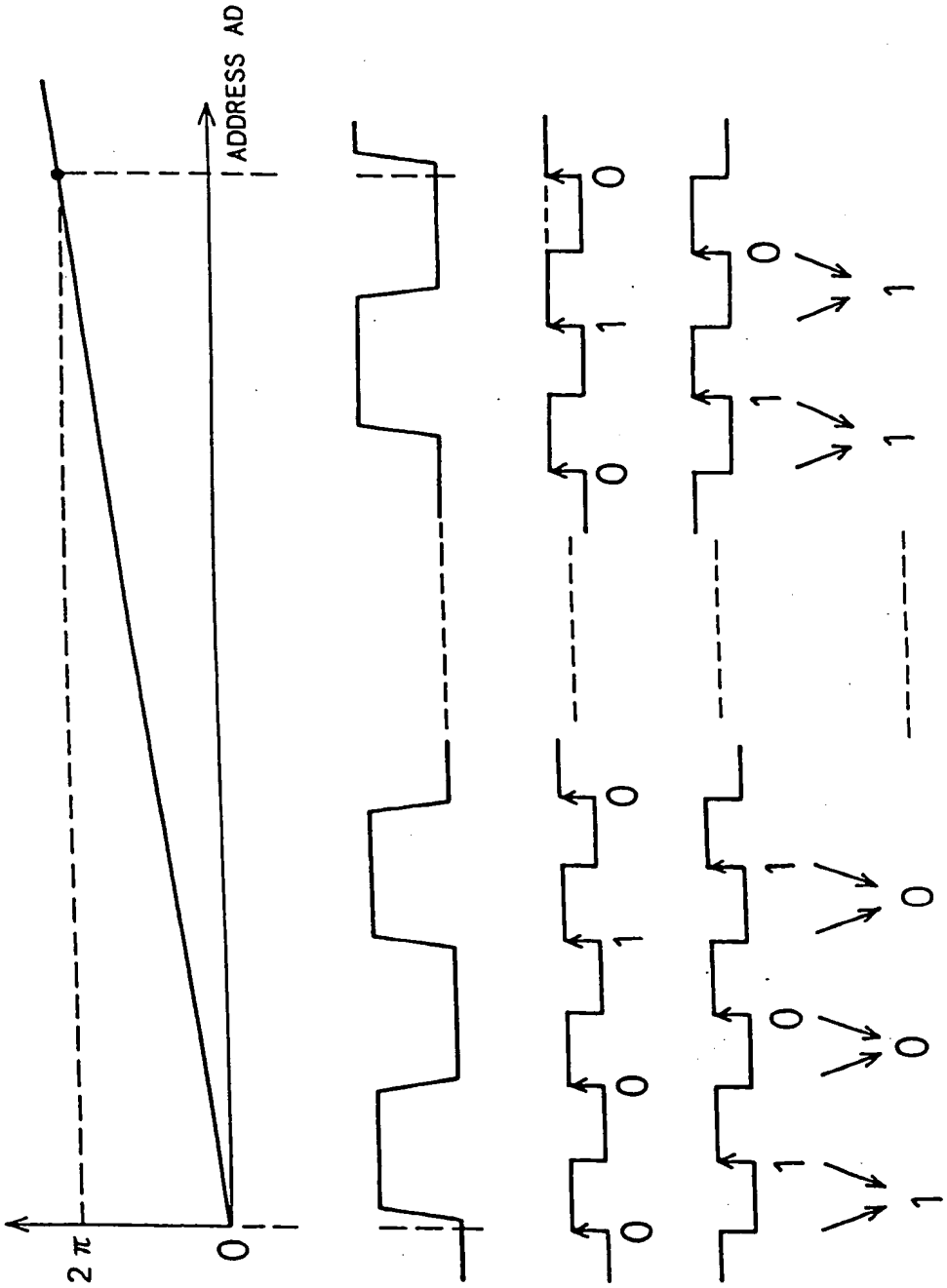



FIG. 37A
PHASE DEVIATION

FIG. 37B
VIDEO SIGNAL 101

FIG. 37C
SAMPLING OF BINARY DATA PF(AD)

FIG. 37D
SAMPLING OF BINARY DATA PG(AD)

FIG. 37E
EX-OR

Fig. 38

INVERTING POINTS OF Q2 (AD)

| NUMBER | INVERTING ADDRESS |
|---|---|
| #1 | 62 |
| #2 | 87 |
| #3 | 173 |
| #4 | 264 |
| #5 | 348 |
| #6 | 430 |
| #7 | 511 |
| #8 | 605 |
| #9 | 680 |
| #10 | 779 |
| #11 | 853 |

Fig. 39

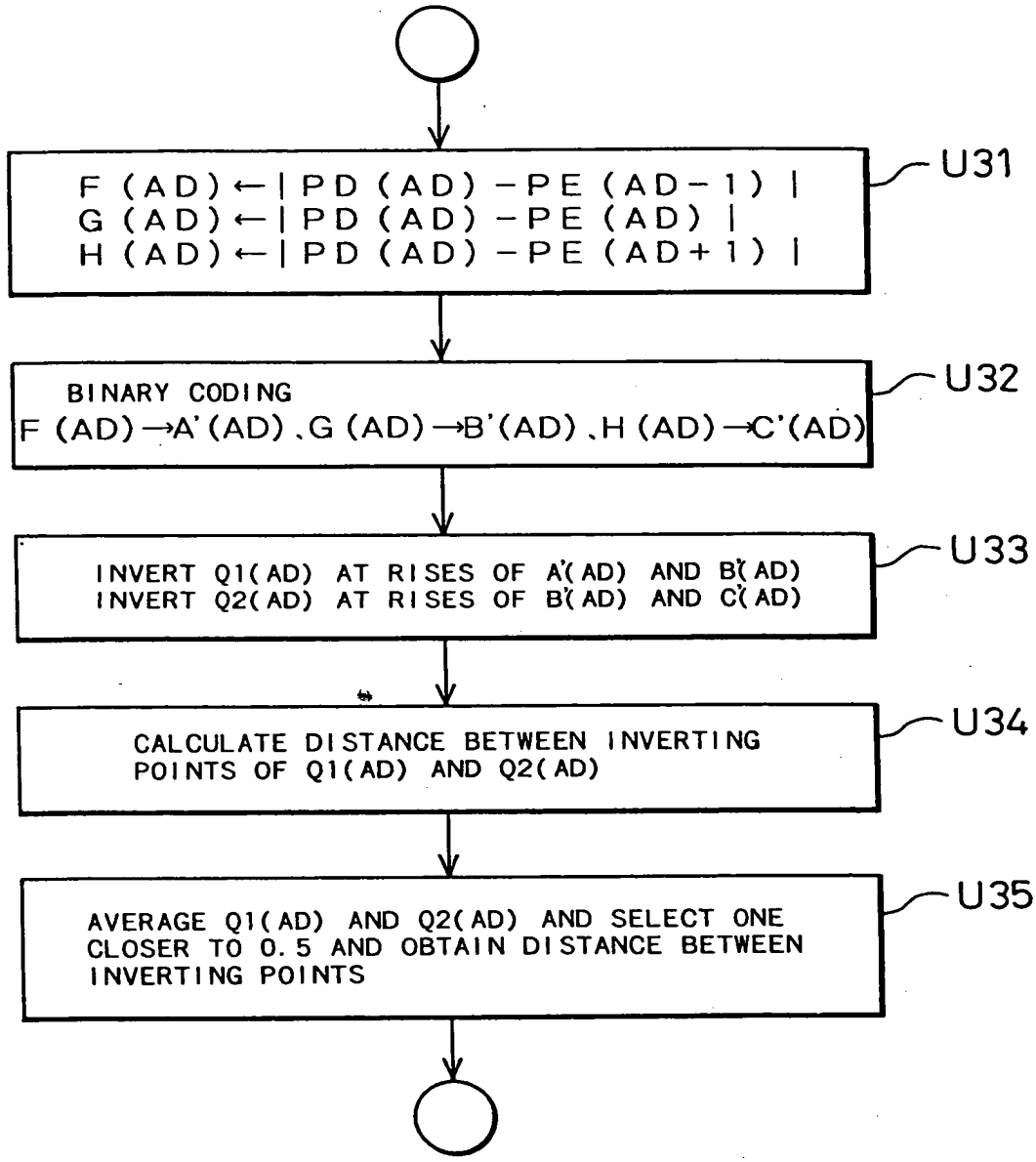
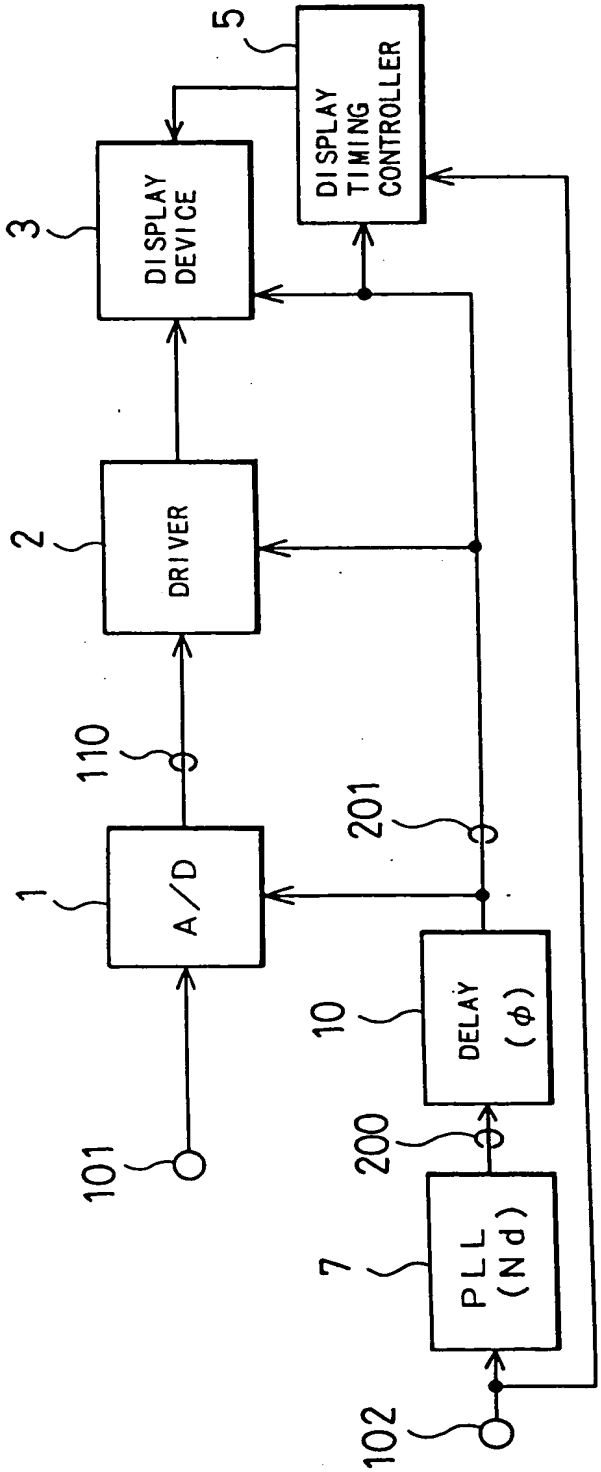

F (AD) ← | PD (AD) − PE (AD − 1) |
G (AD) ← | PD (AD) − PE (AD) |
H (AD) ← | PD (AD) − PE (AD + 1) |
U31
BINARY CODING
F (AD) → A' (AD) , G (AD) → B' (AD) , H (AD) → C' (AD)
U32
INVERT Q1(AD) AT RISES OF A'(AD) AND B'(AD)
INVERT Q2(AD) AT RISES OF B'(AD) AND C'(AD)
U33
CALCULATE DISTANCE BETWEEN INVERTING POINTS OF Q1(AD) AND Q2(AD)
U34
AVERAGE Q1(AD) AND Q2(AD) AND SELECT ONE CLOSER TO 0.5 AND OBTAIN DISTANCE BETWEEN INVERTING POINTS
U35

Fig. 40
*PRIOR ART*



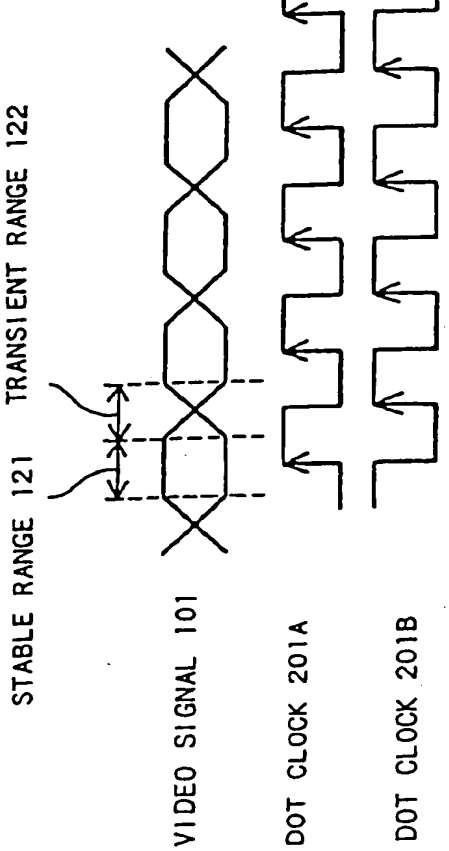



FIG. 41A
PRIOR ART

FIG. 41B
PRIOR ART

FIG. 41C
PRIOR ART

FIG. 42A
PRIOR ART

FIG. 42B
PRIOR ART

FIG. 42C
PRIOR ART

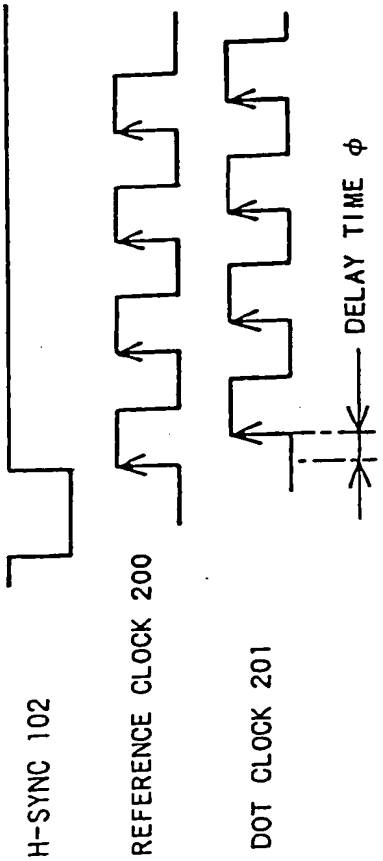
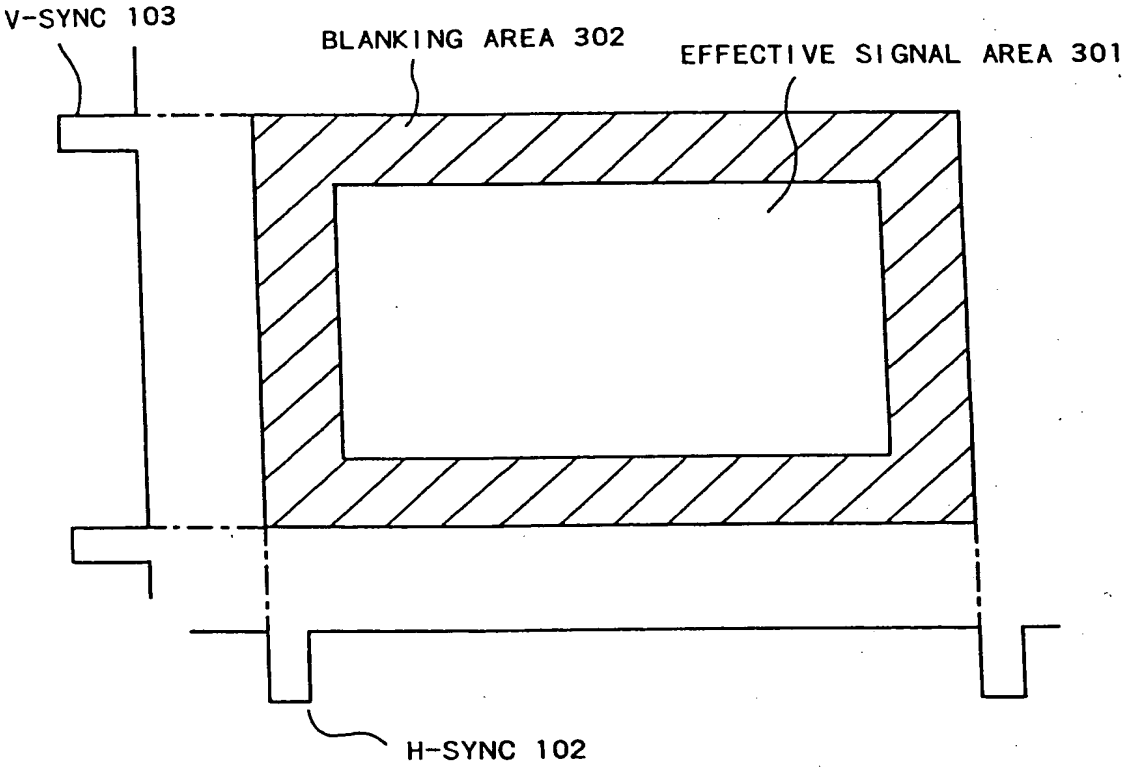


Fig. 43
*PRIOR ART*



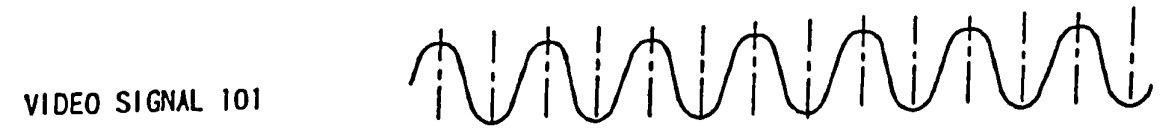



FIG. 44A1
PRIOR ART


FIG. 44A2
PRIOR ART

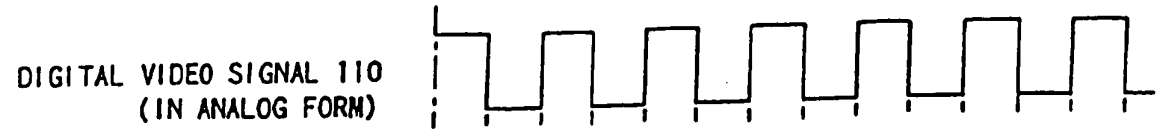



FIG. 44A3
PRIOR ART


FIG. 44B1
PRIOR ART


FIG. 44B2
PRIOR ART

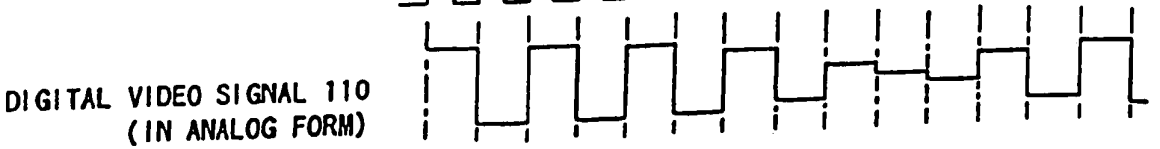



FIG. 44B3
PRIOR ART